

Technical Data sheet

NLN500a

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Preface

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Revision history

| Name | Description of Change | Date | Version |
|-----------------|---|------------|---------|
| Kamesh Lakhwani | Initial version | 07/08/2020 | 1.0 |
| Kamesh Lakhwani | Added Temperature and Humidity data as per the test carried out in Environmental Chamber at SLS | 11/11/2020 | 1.1 |
| Sagar Mistry | Updated RF details | 13/11/2020 | 1.2 |
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Approval

| Name | Position | Signature | Date |
|-----------------------|----------|---|------------|
| Himanshu Ankleshwaria | Manager | Email approval received (must be stored in document library with Approved version) | 13/11/2020 |

Table of Contents

| | |
|---|-----------|
| 1. Introduction..... | 4 |
| 1.1. Brief Specifications..... | 4 |
| 1.2. Block Diagram..... | 4 |
| 2. Different Images of the Module..... | 5 |
| 3. Key Features..... | 6 |
| 4. Applications..... | 6 |
| 5. Specification..... | 7 |
| 5.1. Functional Characteristics..... | 7 |
| 5.1.1. CPU:..... | 7 |
| 5.1.2. Memory:..... | 7 |
| 5.1.3. Clock sources:..... | 7 |
| 5.2. RF Characteristics..... | 7 |
| 5.3. Electrical Characteristic..... | 8 |
| 5.3.1. Absolute Max. Rating..... | 8 |
| 5.3.2. Recommended Operating Conditions..... | 8 |
| 5.3.3. Current Consumption..... | 8 |
| 5.3.4. Environmental Characteristic..... | 8 |
| | 9 |
| 6. Pin Diagram..... | 9 |
| 6.1. Pin Diagram of Module..... | 9 |
| | 9 |
| 6.2.Pin Details of the module..... | 10 |
| 7. Programming Information..... | 12 |
| 8. Reset Information..... | 12 |
| 9. Recommended antenna..... | 13 |
| 10. Soldering Information..... | 13 |
| 11.Package Outline..... | 14 |
| 12. Regulatory Approval..... | 14 |
| | 14 |

1. Introduction

The NebuLink Node NLN500a is First and Smallest STM32WL Based LoRa Module.

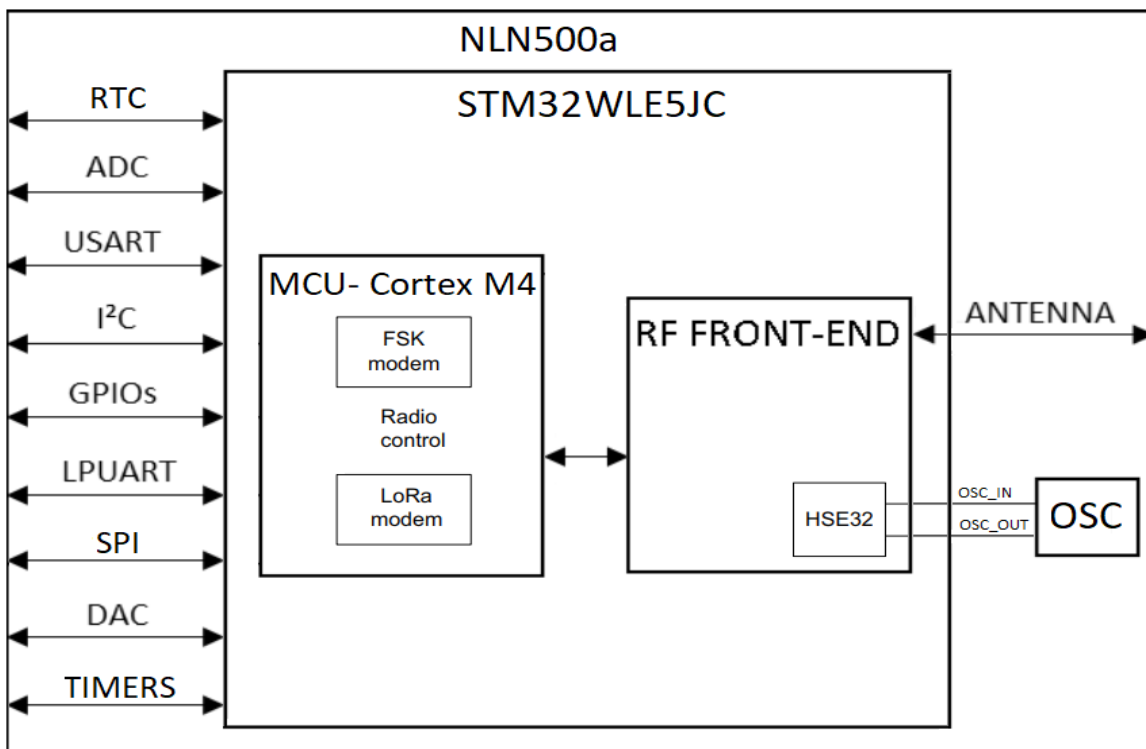
It is build on the STM32WL SoC which has Embedded LoRaWAN Transceiver for wide range of Smart Applications. It is useful when long range is required as it operates at 868 MHz & 915 MHz Band and uses Lo–Ra(Long-Range) and Sigfox Protocol for communication. It offers long range, low power and secure data transmission for M2M and IoT applications.

These Module designed to be extremely low-power and is based on the high-performance STM32WLE5JC Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 48 MHz. This core implements a full set of DSP instructions and an independent memory protection unit (MPU) that enhances the application security.

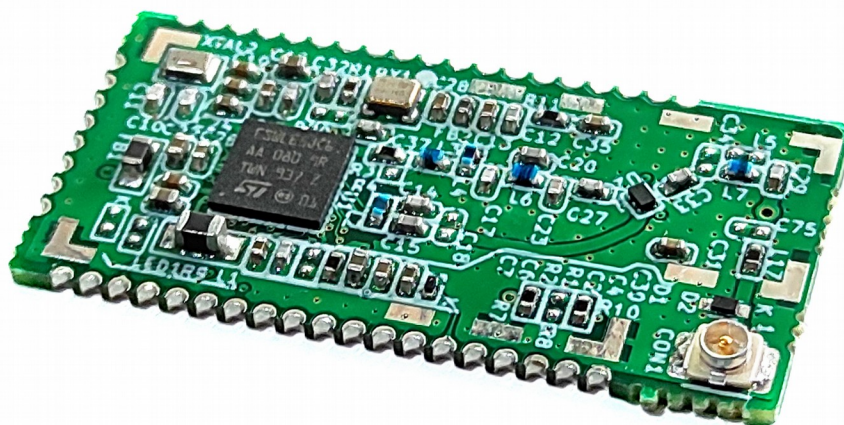
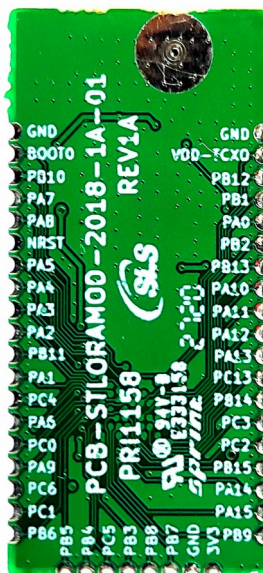
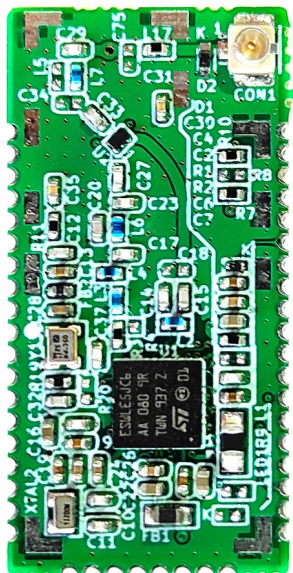
1.1. Brief Specifications

| Module | Chip | Power(dBm) | Antenna | Dimension (mm) LxWxH |
|---------|-------------|------------|----------|----------------------|
| NLN500a | STM32WLE5JC | +21 | External | 16.0×32.6×3.5 |

1.2. Block Diagram



2. Different Images of the Module



3. Key Features

- Frequency Band: Supports EU 863-870,US 902-928,IN865
- RX sensitivity: –122 dBm (125 kHz BW and spreading factor 7) and –136 dBm (125 kHz BW and spreading factor 12) for LoRa
- Transmitter high output power programmable up to +21 dBm
- Its support protocols such as LoRaWAN® and Sigfox™
- 1.8V to 3.6 V power supply
- -20°C to +75 °C operating temperature range
- Core: 32-bit Arm®Cortex®-M4 CPU
- Hardware encryption AES 256-bit
- OTA(over-the-air) firmware update capable
- Up to 256-Kbyte Flash memory
- Up to 64-Kbyte RAM
- Serial-wire debug (SWD), JTAG for the application processor
- Up to 43 I/Os, most 5 V-tolerant available on Edge Plated holes of the module
- The Module can be directly soldered on any device board
- RF shield on the module for preventing the module from external electromagnetic radiation and interference

4. Applications

The applications include, but are not limited to:

- Building automation & monitoring
- Lighting controls
- Inventory management
- Environmental monitoring
- Security
- Industrial monitoring

- Machinery condition and performance monitoring
- Monitoring of plant system parameters such as temperature, pressure, flow, tank level, humidity, vibration, etc.
- Smart Metering & Lighting Solutions
- Smart Flood Sensors
- Smart Street Lighting
- Smart City Network
- Smart Waste Management, etc.

5. Specification

5.1. Functional Characteristics

5.1.1. CPU:

- High-performance STM32WLE5JC Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 48 MHz.

5.1.2. Memory:

- Up to 256-Kbyte Flash memory
- Up to 64-Kbyte RAM

5.1.3. Clock sources:

- External HSE Clock 32 MHz TCXO
- External 32 kHz oscillator for RTC with calibration

5.2. RF Characteristics

| Parameter | NLN500a |
|------------------------------|--|
| Transmit Power | +21 dBm |
| Receive Sensitivity (1% PER) | -122 dBm (125 kHz BW, spreading factor 7) and -136 dBm (125 kHz BW, spreading factor 12) |
| RF Range(Line-Of-Sight) | 10KM* |
| Frequency Band | EU 863-870,US 902-928,IN865 |
| RF Data Rate | 0.013 to 17.4 Kbit/s |

Note:

*Range figure estimates are based on ideal conditions with limited sources of interference. Actual range will vary based on transmitting power, type of transmitting antenna used, height of transmitting antenna, height of receiving antenna, orientation of transmitter and receiver, weather conditions, interference sources in the area, and terrain between receiver and transmitter.

5.3. Electrical Characteristic

5.3.1. Absolute Max. Rating

| Symbol | Description | Min | Max | Unit |
|------------|---|------|------|------|
| VDDX - VSS | External main supply voltage (including VDD, VDDA, VDDRF, VDDSMPS, VBAT, VREF+) | -0.3 | +3.9 | V |

5.3.2. Recommended Operating Conditions

| Symbol | Description | Min | Typ | Max | Units |
|--------|----------------------------|-----|-----|-----|-------|
| VDD | Standard operating voltage | 1.8 | 3.3 | 3.6 | V |

5.3.3. Current Consumption

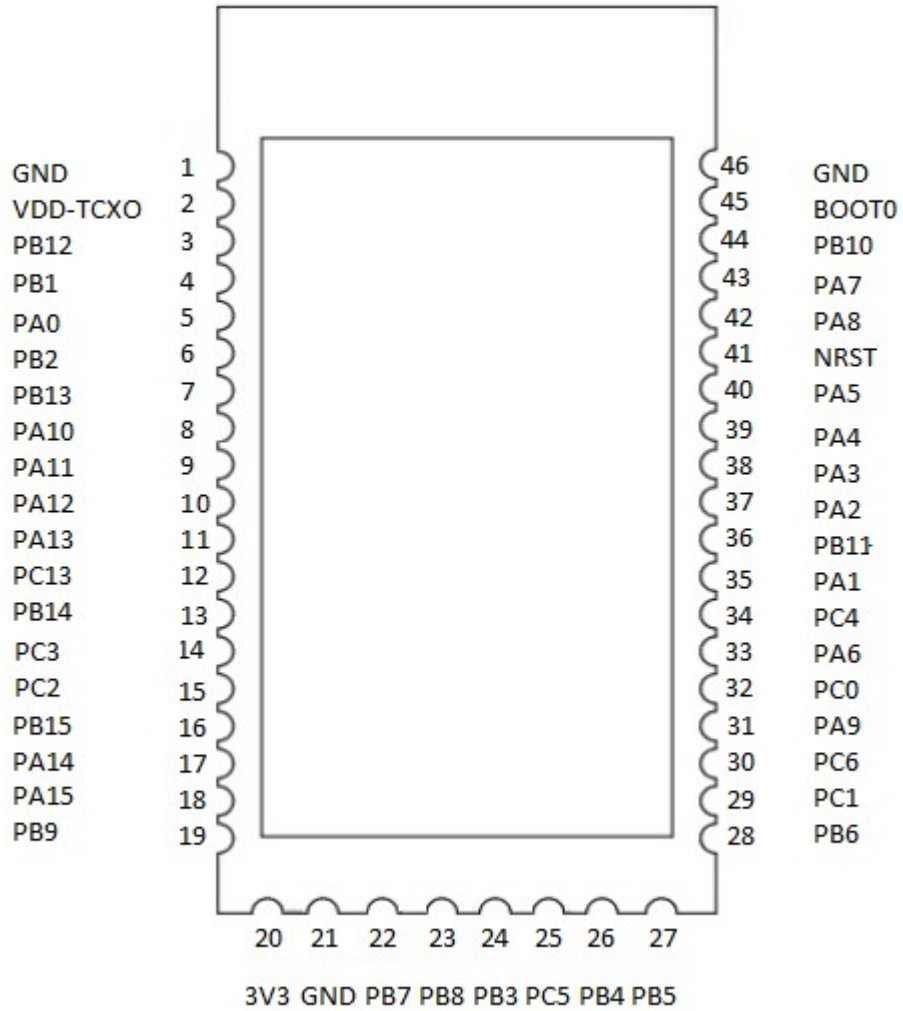
| Mode | Current | Condition |
|----------------------|---------|--|
| Radio in transmit | 132mA | 868 MHz, +21 dBm, 3.3 V,SF7,125KHz |
| | 130mA | 868 MHz, +21 dBm, 3.3 V,SF12,125KHz |
| Radio in receive | 10mA | Rx boosted, LoRa 125 kHz, SMPS ON |
| Standby (RTC enable) | 1.6μA | VDD = 3 V |
| Deep-Sleep mode | 1μA | Sleep with cold start (All blocks off) |

5.3.4. Environmental Characteristic

- Operating Temperature: -20 °C to 75 °C
- Humidity: 95%

6. Pin Diagram

6.1. Pin Diagram of Module



6.2.Pin Details of the module

| Pin # | Pin Name | Pin Type | Pin Function/Alternate Functions |
|-------|--------------|----------|--|
| 1 | GND | S | Ground |
| 2 | PB0-VDD-TCXO | I/O | COMP1_OUT, CM4_EVENTOUT |
| 3 | PB12 | I/O | TIM1_BKIN, I2C3_SMBA, SPI2_NSS/I2S2_WS, LPUART1_RTS, CM4_EVENTOUT |
| 4 | PB1 | I/O | LPUART1_RTS_DE, LPTIM2_IN1, CM4_EVENTOUT |
| 5 | PA0 | I/O | TIM2_CH1, I2C3_SMBA, I2S_CKIN, USART2_CTS, COMP1_OUT, TIM2_ETR, CM4_EVENTOUT |
| 6 | PB2 | I/O | LPTIM1_OUT, I2C3_SMBA, SPI1_NSS, DEBUG_RF_SMPSRDY, CM4_EVENTOUT |
| 7 | PB13 | I/O | TIM1_CH1N, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_CTS, CM4_EVENTOUT |
| 8 | PA10 | I/O | RTC_REFIN, TIM1_CH3, I2C1_SDA, SPI2_MOSI/I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT |
| 9 | PA11 | I/O | TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_NRESET, CM4_EVENTOUT |
| 10 | PA12 | I/O | TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT |
| 11 | PA13 | I/O | JTMS-SWDIO, I2C2_SMBA, IR_OUT, CM4_EVENTOUT |
| 12 | PC13 | I/O | CM4_EVENTOUT |
| 13 | PB14 | I/O | TIM1_CH2N, I2S2_MCK, I2C3_SDA, SPI2_MISO, CM4_EVENTOUT |
| 14 | PC3 | I/O | LPTIM1_ETR, SPI2_MOSI/I2S2_SD, LPTIM2_ETR, CM4_EVENTOUT |
| 15 | PC2 | I/O | LPTIM1_IN2, SPI2_MISO, CM4_EVENTOUT |
| 16 | PB15 | I/O | TIM1_CH3N, I2C2_SCL, SPI2_MOSI/I2S2_SD, CM4_EVENTOUT |
| 17 | PA14 | I/O | JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT |

| | | | |
|----|------|-----|--|
| 18 | PA15 | I/O | JTDI, TIM2_CH1, TIM2_ETR, I2C2_SDA, SPI1_NSS, CM4_EVENTOUT |
| 19 | PB9 | I/O | TIM1_CH3N, I2C1_SDA, SPI2_NSS/I2S2_WS, IR_OUT, TIM17_CH1, CM4_EVENTOUT |
| 20 | 3V3 | S | Module Supply |
| 21 | GND | S | Ground |
| 22 | PB7 | I/O | LPTIM1_IN2, TIM1_BKIN, I2C1_SDA, USART1_RX, TIM17_CH1N, CM4_EVENTOUT |
| 23 | PB8 | I/O | TIM1_CH2N, I2C1_SCL, RF_IRQ2, TIM16_CH1, CM4_EVENTOUT |
| 24 | PB3 | I/O | JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, RF_IRQ0, USART1_RTS, CM4_EVENTOUT |
| 25 | PC5 | I/O | CM4_EVENTOUT |
| 26 | PB4 | I/O | NJTRST, I2C3_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_LDORDY, TIM17_BKIN, CM4_EVENTOUT |
| 27 | PB5 | I/O | LPTIM1_IN1, I2C1_SMBA, SPI1_MOSI, RF_IRQ1, USART1_CK, COMP2_OUT, TIM16_BKIN, CM4_EVENTOUT |
| 28 | PB6 | I/O | LPTIM1_ETR, I2C1_SCL, USART1_TX, TIM16_CH1N, CM4_EVENTOUT |
| 29 | PC1 | I/O | LPTIM1_OUT, SPI2_MOSI/I2S2_SD, I2C3_SDA, LPUART1_TX, CM4_EVENTOUT |
| 30 | PC6 | I/O | I2S2_MCK, CM4_EVENTOUT |
| 31 | PA9 | I/O | TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX, CM4_EVENTOUT |
| 32 | PC0 | I/O | LPTIM1_IN1, I2C3_SCL, LPUART1_RX, LPTIM2_IN1, CM4_EVENTOUT |
| 33 | PA6 | I/O | TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_MISOOUT, TIM16_CH1, CM4_EVENTOUT |
| 34 | PC4 | I/O | CM4_EVENTOUT |
| 35 | PA1 | I/O | TIM2_CH2, LPTIM3_OUT, I2C1_SMBA, SPI1_SCK, USART2_RTS, LPUART1_RTS, CM4_EVENTOUT |
| 36 | PB11 | I/O | TIM2_CH4, I2C3_SDA, LPUART1_TX, COMP2_OUT, CM4_EVENTOUT |
| 37 | PA2 | I/O | LSCO, TIM2_CH3, USART2_TX, |

| | | | |
|----|-------|-----|---|
| | | | LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT |
| 38 | PA3 | I/O | TIM2_CH4, I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT |
| 39 | PA4 | I/O | RTC_OUT2, LPTIM1_OUT, SPI1_NSS, USART2_CK, DEBUG_SUBGHZSPI_NSSOUT, LPTIM2_OUT, CM4_EVENTOUT |
| 40 | PA5 | I/O | TIM2_CH1, TIM2_ETR, SPI2_MISO, SPI1_SCK, DEBUG_SUBGHZSPI_SCKOUT, LPTIM2_ETR, CM4_EVENTOUT |
| 41 | NRST | I/O | Reset |
| 42 | PA8 | I/O | MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT |
| 43 | PA7 | I/O | TIM1_CH1N, I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_MOSIOUT, TIM17_CH1, CM4_EVENTOUT |
| 44 | PB10 | I/O | TIM2_CH3, I2C3_SCL, SPI2_SCK/I2S2_CK, LPUART1_RX, COMP1_OUT, CM4_EVENTOUT |
| 45 | BOOT0 | I/O | CM4_EVENTOUT |
| 46 | GND | S | Ground |

7. Programming Information

It can be programmed using STLink or STM32F446 Nucleo-64 programmer board with below pin interface.

1. GND
2. 3V3
3. JTMS-SWDIO (PA13)
4. JTCK-SWCLK (PA14)
5. NRST

8. Reset Information

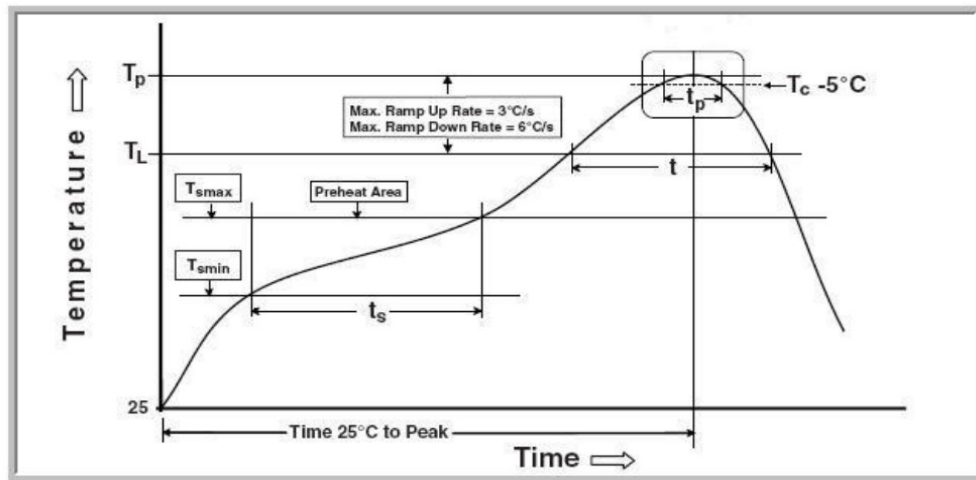
NRST is maintained HIGH in module itself. This pin is active low.

9. Recommended antenna

Any 50 ohm matched antenna with U.FL connection.

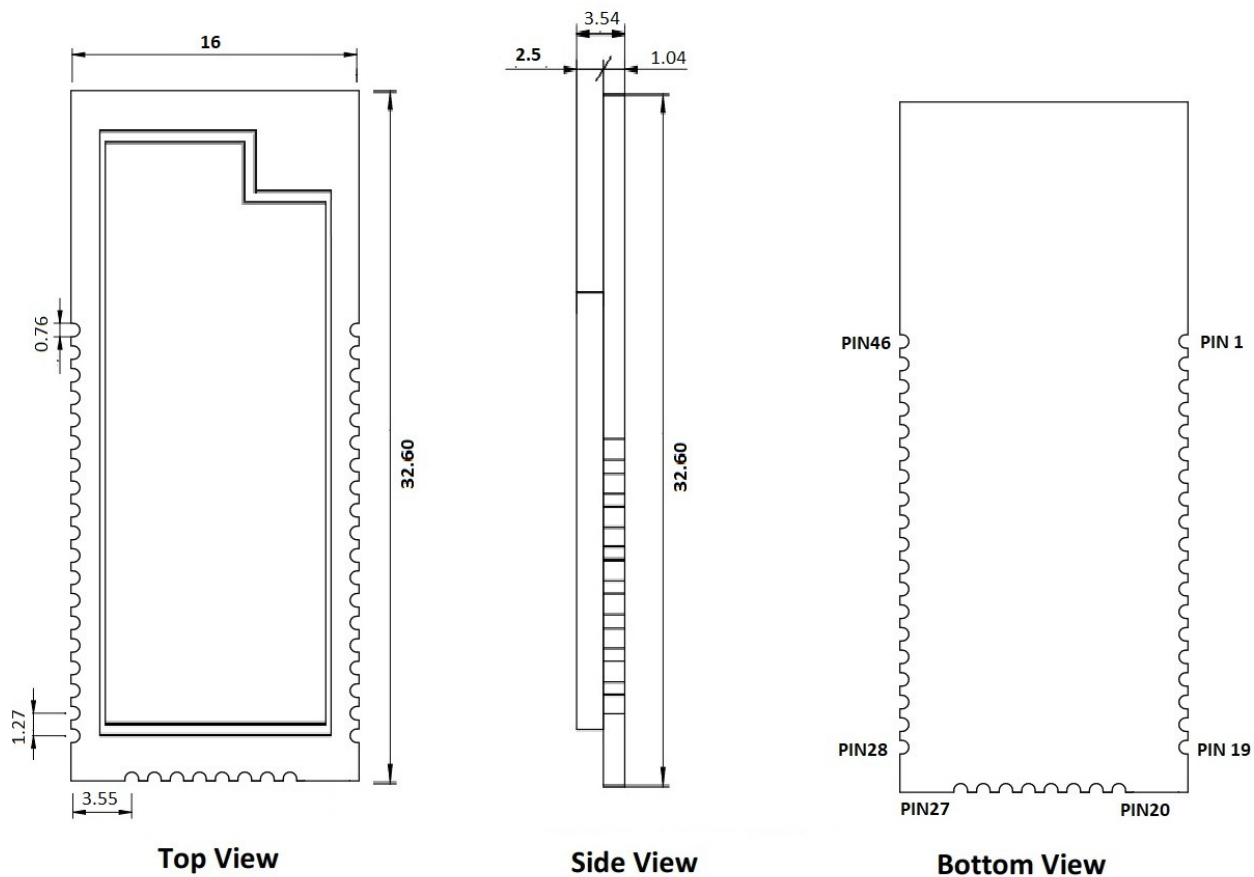
10. Soldering Information

For reflow soldering, it is recommended to follow the reflow profile in below figure as a guide, as well as the paste manufacturer's guidelines on peak flow temperature, soak times, time above liquid and ramp rates.



| Profile Feature | Pb-Free Assembly |
|---|----------------------------------|
| Average Ramp-Up Rate (T _{Smax} to T _P) | 3°C / second max. |
| Preheat Temperature Min (T _{Smin}) Temperature Max (T _{Smax}) Time (t _{Smin} to t _{Smax}) | 150°C 200°C 60-180 seconds |
| Time maintained above Temperature (T _L) Time (t _L) | 217°C 60-150 seconds |
| Peak/Classification Temperature (T _P) | 245°C |
| Time within 5°C of the specified Peak Temperature (t _P) | 20-40 seconds |
| Ramp-Down Rate (T _P to T _L) | 6°C / second max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

11. Package Outline



Note: All dimensions are in mm.

12. Regulatory Approval

| | |
|--------------------|---------------|
| CE-RED | Under Process |
| FCC | Under Process |
| WEEE | Under Process |
| RoHS | Under Process |
| LoRa Certification | Under Process |
| WPC | Under Process |