

USB 2.0 OTG Transceiver with ULPI Interface

1. General Description

The RN1133 is a high performance USB 2.0 transceiver chip which supports low speed (LS), full speed (FS) and high speed (HS) data rates. The interface to a link controller is via the UTMI+ Low Pin Interface (ULPI).

RN1133 also supports the on-the-go (OTG) mode which allows both Host and Peripheral operations. An up to 8kV HBM ESD protection circuit is integrated to the USB connection pins providing stronger ESD protection while reducing BOM at the same time. With the built-in 3.3V to 1.8V regulator and power on reset circuit, RN1133 is the best choice in terms of both performance and cost for USB 2.0 OTG transceiver applications.

2. Ordering Information

RN1133 □ □



Package Type

QW : WQFN-32L 5x5 (W-Type)

Operating Temperature Range

E : Pb Free with Industrial Standard

G: Green (Halogen Free with
Commercial Standard)

Note :

Richnex Pb-free and Green products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

3. Features

- Complies with *Universal Serial Bus Specification Rev. 2.0*.
- USB-IF OTG Compliance Test certified. TID: 100000021.
- Compatible with *USB On-The-Go Supplement Rev. 1.3*.
- Complies with *UTMI+ Low Pin Interface (ULPI) Rev. 1.1*.
- Complies with ULPI 8 bit mode.
- Supports ULPI 3/6 bit serial interface modes.
- Supports the USB Host Negotiation Protocol (HNP) and Session Control Protocol (SRP).
- Supports USB FS pre-amble packets.
- Supports Carkit Mode which routes UART signals thru USB pins.
- Integrated 24MHz crystal oscillator allows both crystal and input clock operations.
- Only requires a single 3.3V power supply with an integrated 3.3V to 1.8V LDO.
- +/- 8kV ESD protection on DP, DM and ID pins.
- Integrated Power On Reset circuit.
- Low power consumption and suspend current for portable applications.
- Small footprint (5mm x 5mm) 32-pin QFN package.

4. Applications

- GPS Navigators
- Network Routers
- Smartphones
- Network Attached Storages (NAS)

Table of Contents

1. General Description	1
2. Ordering Information	1
3. Features	1
4. Applications	1
5. Block Diagram	5
6. Pin Diagram	6
7. Pin Description	7
8. Function Description	8
8.1 ULPI Interface.....	8
8.1.1 Synchronous Mode	9
8.1.2 Low Power Mode	16
8.1.3 6-Pin FsLs Serial Mode.....	17
8.1.4 3-Pin FsLs Serial Mode.....	18
8.1.5 Carkit Mode.....	18
8.2 PLL and Crystal Oscillator	19
8.3 Reference and Bias	19
8.4 1.8V Voltage Regulator.....	19
8.5 Power On Reset	19
8.6 OTG	20
8.6.1 ID Detect.....	20
8.6.2 VBUS Comparator	21
8.7 USB Transceiver/CDR	21
9. ULPI Registers	22
9.1 Register Map	22
9.1.1 Vendor ID and Product ID	23
9.1.2 Function Control.....	23
9.1.3 Interface Control	24
9.1.4 OTG Control.....	26
9.1.5 USB Interrupt Enable Rising	27
9.1.6 USB Interrupt Enable Falling	28
9.1.7 USB Interrupt Status	28
9.1.8 USB Interrupt Latch	29
9.1.9 Debug	30
9.1.10 Scratch.....	30
9.1.11 Carkit Control	31

9.1.12 Carkit Interrupt Enable	31
9.1.13 Carkit Interrupt Status	32
9.1.14 Carkit Interrupt Latch	32
9.1.15 Reserved.....	32
9.2 Register Settings for All Upstream and Downstream Signaling Modes.....	33
10. Electrical Characteristics.....	35
11. Absolute Maximum Ratings.....	37
12. Recommended Operating Conditions	37
13. Typical Application Diagram	38
14. Package Outline.....	39
15. Datasheet Revision History	40

List of Figures

Figure 1. RN1133 Block Diagram.....	5
Figure 2. RN1133 Pin Diagram	6
Figure 3. ULPI Synchronous Mode Timing	10
Figure 4. RegWrite Operation	13
Figure 5. RegRead Operation	14
Figure 6. USB Packet Transmit in HS	14
Figure 7. USB Packet Transmit in FS/LS	15
Figure 8. USB Packet Receive in HS	15
Figure 9. USB Packet Receive in FS/LS	16
Figure 10. Enter Low Power Mode.....	17
Figure 11. Exit Low Power Mode	17
Figure 12. Power On Reset Sequence	20
Figure 13. Typical Application Diagram.....	38
Figure 14. Package Outline.....	39

List of Tables

Table 1. RN1133 Pin Definition	7
Table 2. ULPI Synchronous Mode Pin Definition	9
Table 3. ULPI Synchronous Mode Timing	10
Table 4. TX CMD Byte Definition.....	11
Table 5. RX CMD Definition	11
Table 6. Low Power Mode Pin Definition.....	16
Table 7. 6-Pin FsLs Serial Mode Pin Definition	18
Table 8. 3-Pin FsLs Serial Mode Pin Definition	18

Table 9. Carkit Mode Pin Definition	18
Table 10. ID Pin Detection Combination	21
Table 11. Register Table	22
Table 12. VID/PID Register	23
Table 13. Function Control Register.....	23
Table 14. Interface Control Register.....	24
Table 15. OTG Control Register.....	26
Table 16. USB Interrupt Enable Rising Register	27
Table 17. USB Interrupt Enable Falling Register.....	28
Table 18. USB Interrupt Status Register	28
Table 19. USB Interrupt Latch Register.....	29
Table 20. USB Interrupt Latch Register Rule	30
Table 21. Debug Register.....	30
Table 22. Scratch Register	30
Table 23. Carkit Control Register	31
Table 24. Carkit Interrupt Enable Register	31
Table 25. Carkit Interrupt Status Register	32
Table 26. Carkit Interrupt Latch Register.....	32
Table 27. Register Setting for All Signaling Mode	33
Table 28. Electrical Characteristics	35
Table 29. Absolute Maximum Ratings	37
Table 30. Recommended Operating Conditions.....	37
Table 31. Datasheet Revision History	40

5. Block Diagram

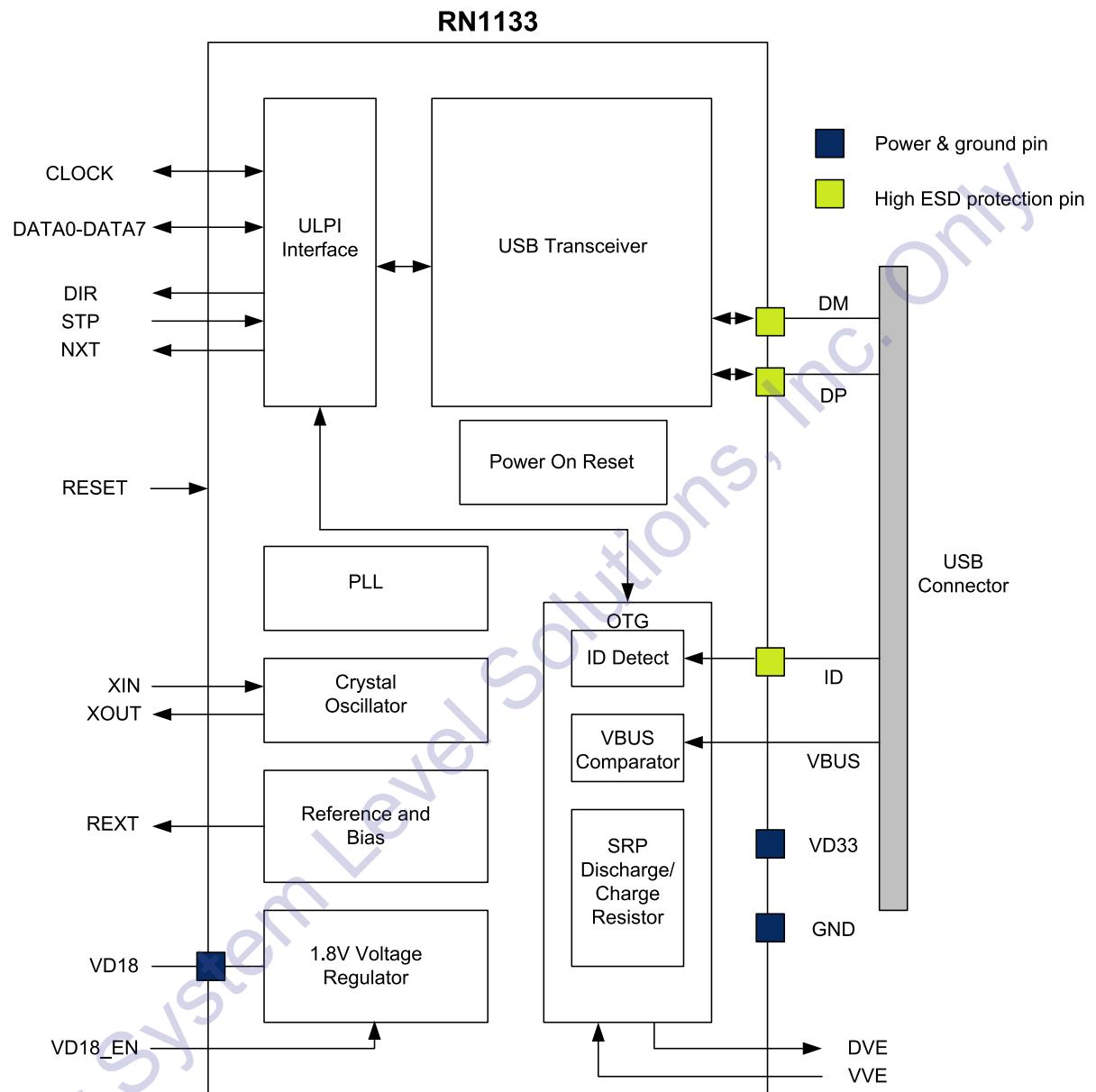


Figure 1. RN1133 Block Diagram

6. Pin Diagram

Figure 2 shows the pin definitions and locations of RN1133's QFN32 package (top view)

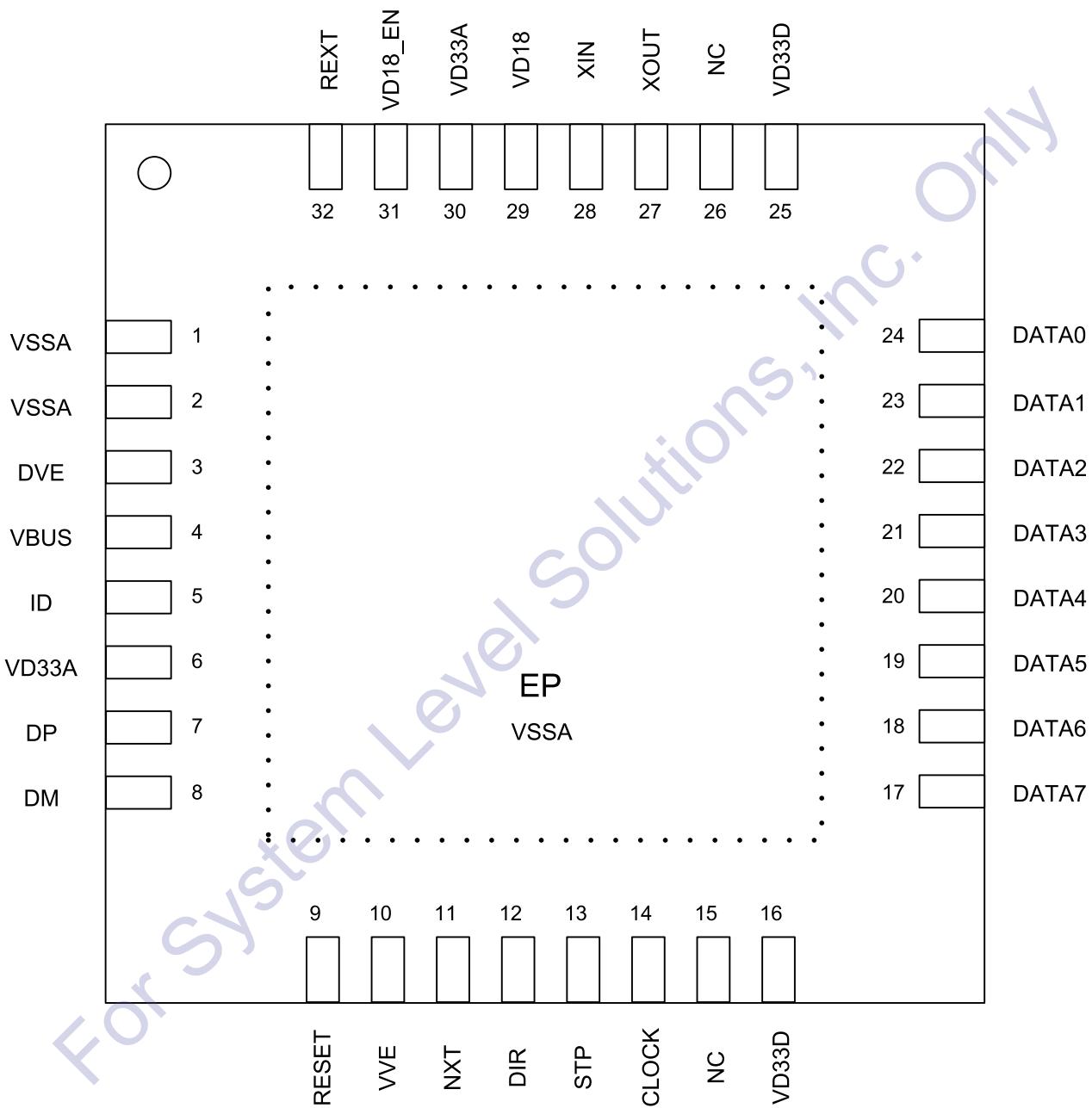


Figure 2. RN1133 Pin Diagram

7. Pin Description

Table 1. RN1133 Pin Definition

Symbol	Pin	Type	Reset State	Description
CLOCK	14	O	L	CLOCK - 60MHz ULPI clock. All interface signals are synchronous to CLOCK.
DATA0	24	IO	L	DATA[0-7] - ULPI bidirectional data bus, driven low by the Link during idle. Bus ownership is determined by DIR. The interface protection circuit for DATA[0-7] can be enabled via the InterfaceProtectDisable bit in the Interface Control register.
DATA1	23			
DATA2	22			
DATA3	21			
DATA4	20			
DATA5	19			
DATA6	18			
DATA7	17			
DIR	12	O	H	Direction - Controls directions of ULPI bus DATA0-DATA7. The RN1133 drives DIR high to take ownership of the bus or to indicate it can not accept data from the Link. The RN1133 drives DIR low when it has no data to transfer.
STP	13	I		Stop - The Link asserts this signal for one clock cycle to stop the data stream currently on the ULPI bus. The interface protection circuit for STP can be enabled via the InterfaceProtectDisable bit in the Interface Control register.
NXT	11	O	L	Next -The RN1133 asserts this signal to throttle the data.
DVE	3	O	H	Drive VBUS External – High active. This signal enables the external VBUS power switch.
VVE	10	I		VBUS Valid External - This signal should be connected to FAULT output of the external VBUS power switch or the external VBUS valid comparator. The integrated pull down register prevents floating when the external power switch/comparator is not used.
RESET	9	I		Asynchronous chip reset - High active. This signal is equivalent to the RESET bit in the Function Control register. The integrated pull-down resistor prevents floating when this pin is not connected.
XIN	28	I		Crystal in – 24 MHz crystal oscillator input. An external clock source can also be applied to this pin in place of the crystal.

Symbol	Pin	Type	Reset State	Description
XOUT	27	O		Crystal out – 24/19.2 MHz crystal oscillator output. This pin should not be connected when the external clock source is used.
VD18_EN	31	I		Internal 1.8V voltage regulator enable. It should be connected to pin 30 to enable the internal 1.8V regulator and be connected to ground to disable the internal 1.8V regulator. External 1.8V should be applied to VD18 pin when the internal 1.8V regulator is disabled.
REXT	32	A		Bias current setting resistor pin. It should be connected to a 20K Ohm resistor to ground.
VD18	29	A		1.8V internal regulator output.
VBUS	4	A		USB VBUS. The pin is used for the VBUS Comparator input and SRP charging/discharging.
ID	5	A		USB ID. This pin should be 0 for an OTG A-Device and 1 for an OTG B-Device. For non-OTG applications, the pin can be floated.
DM	8	A		USB D-.
DP	7	A		USB D+.
VD33A	6, 30	A		3.3V power for analog blocks.
VD33D	16,25	A		3.3V power for digital blocks.
VSSA	1, 2	A		Ground pin for analog blocks.
NC	15, 26	NC		No connection. Reserved for future usage.
VSSD	EP	A		Ground pin for digital blocks (including 1.8V, 3.3V digital circuitry).
Note: EP - Exposed Paddle (bottom of the package) to be connected to board ground plane.				

8. Function Description

8.1 ULPI Interface

The RN1133's 12 pin ULPI interface is compliant with the industrial standard UTMI+ Low Pin Interface (ULPI) Specification Rev1.1 and provides a glueless interface to the Link processor. The RN1133's ULPI compliant register set allows the Link to transmit and receive USB data, control over USB host, OTG, peripheral functionalities, and select the operation mode. An external VBUS power switch can also be controlled via the ULPI register for USB VBUS monitoring, charging and discharging required in the OTG operation. The RN1133's ULPI interface can be configured into Synchronous, Low Power, 6-Pin FsLsSerial, 3-Pin FsLsSerial and Carkit modes for various applications.

8.1.1 Synchronous Mode

This is the default mode of operation. While the clock is running and stable, the ULPI interface carries commands and data that are synchronous to CLOCK. Table 2 shows the signal definition of Synchronous Mode.

Table 2. ULPI Synchronous Mode Pin Definition

Signal	Direction	Description
CLOCK	OUT	60MHz interface clock. All interface signals are synchronous to CLOCK.
DATA[7:0]	I/O	Bi-directional data bus. Driven low by the Link during idle. Bus ownership is determined by DIR. The Link and RN1133 initiate data transfers by driving a non-zero pattern onto the data bus. The single edged data is transferred with respect to rising edge of CLOCK.
DIR	OUT	Direction. Controls the direction of the DATA bus. When the RN1133 has data to transfer to the Link, it drives DIR high to take ownership of the bus. When the RN1133 has no data to transfer it drives DIR low and monitors the bus for Link activity. The RN1133 drives DIR high whenever the interface cannot accept data from the Link.
STP	IN	Stop. The Link asserts this signal for 1 clock cycle to stop the data stream currently on the bus. If the Link is sending data to the RN1133, STP indicates the last byte of data was on the bus in the previous cycle. If the RN1133 is sending data to the Link, STP forces the RN1133 to end its transfer, de-assert DIR and relinquish control of the data bus to the Link.
NXT	OUT	Next. The RN1133 asserts this signal to throttle the data. When the Link is sending data to the RN1133, NXT indicates when the current byte has been accepted by the RN1133. The Link places the next byte on the data bus in the following clock cycle. When the RN1133 is sending data to the Link, NXT indicates when a new byte is available for the Link to consume.

Control and data timings for the Synchronous Mode are shown in Figure 3 and Table 3. All timings are measured with respect to the CLOCK signal and are always clocked on the rising edge of CLOCK.

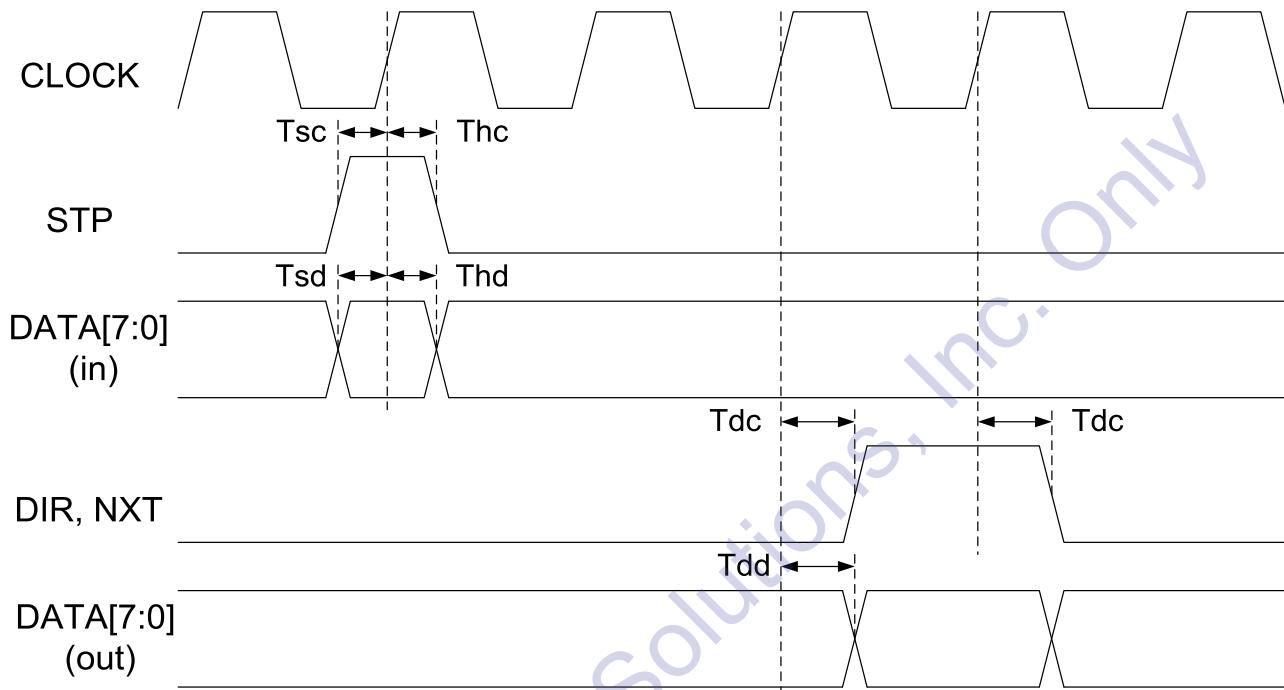


Figure 3. ULPI Synchronous Mode Timing

Table 3. ULPI Synchronous Mode Timing

Parameter	Symbol	Min	Max	Units
Setup time	Tsc, Tsd	6.0		ns
Hold time	Thc, Thd	0.0		ns
Output delay	Tdc, Tdd		5.0	ns

The RN1133's ULPI interface supports the protocol in which a **Transmit Command (TXCMD)** byte that is sent by the Link and a **Receive Command (RXCMD)** byte that is sent by RN1133. Tables 4 and 5 show the structure of the **Transmit Command (TXCMD)** byte and the **Receive Command (RXCMD)** byte:

Table 4. TX CMD Byte Definition

Byte Name	Command code data[7:6]	Command Payload data[5:0]	Command Description
Special	00b	000000b (NOOP)	No operation. 00h is the idle value of the data bus. The Link drives NOOP by default.
		XXXXXXb (RSVD)	Reserved command space.
Transmit	01b	000000b (NOPID)	Transmits USB data that does not have a PID, such as chirp and resume signaling. The RN1133 starts transmitting on the USB bus beginning with the next data byte.
		00XXXXb (PID)	Transmits USB packet. Data[3:0] indicates USB packet identifier PID[3:0].
		XXXXXXb (RSVD)	Reserved command space.
RegWrite	10b	101111b (EXTW)	Extended register write command. 8-bit address available in the next cycle.
		XXXXXXb (REGW)	Register write command with 6-bit immediate address.
RegRead	11b	101111b (EXTR)	Extended register read command. 8-bit address available in the next cycle.
		XXXXXXb (REGR)	Register read command with 6-bit immediate address.

Table 5. RX CMD Definition

Data	Name	Description and Value
1:0	LineState	LineState signals.
		DATA[0] = LineState[0]
		DATA[1] = LineState[1]

Data	Name	Description and Value						
3:2	VBUS State	Encoded VBUS Voltage State						
		Value	V _{BUS} Voltage	SessEnd	SessValid	VbusValid		
		00	V _{BUS} < V _{B_SESS_END}	1	0	0		
		01	V _{B_SESS_END} <= V _{BUS} < V _{SESS_VLD}	0	0	0		
		10	V _{SESS_VLD} <= V _{BUS} < V _{A_VBUS_VLD}	X	1	0		
		11	V _{A_VBUS_VLD} <= V _{BUS}	X	X	1		
5:4	RxEvent	Encoded USB Event Signals						
		Value	RxActive	RxError	HostDisconnect			
		00	0	0	0			
		01	1	0	0			
		11	1	1	0			
		10	X	X	1			
6	ID	Set to the value of IdGnd.						
7	Alt_int	Asserted when a non-USB interrupt occurs. This bit must be set when an unmasked event occurs on any bit in the Carkit Interrupt Latch register. The Link must read the Carkit Interrupt Latch register to determine the source of the interrupt.						

The Link accesses immediate registers by sending the TX CMD first either as a RegWrite or a RegRead command with the required register address.

Figure 4 shows for a register write operation, the Link sends a RegWrite command and waits for NXT to assert. In the cycle after NXT asserts, the Link sends the register write data and waits for NXT to assert again. When NXT asserts the second time, the Link asserts STP in the following cycle to complete the operation. If the RN1133 aborts the RegWrite by asserting DIR, the Link must retry the RegWrite when the bus is idle.

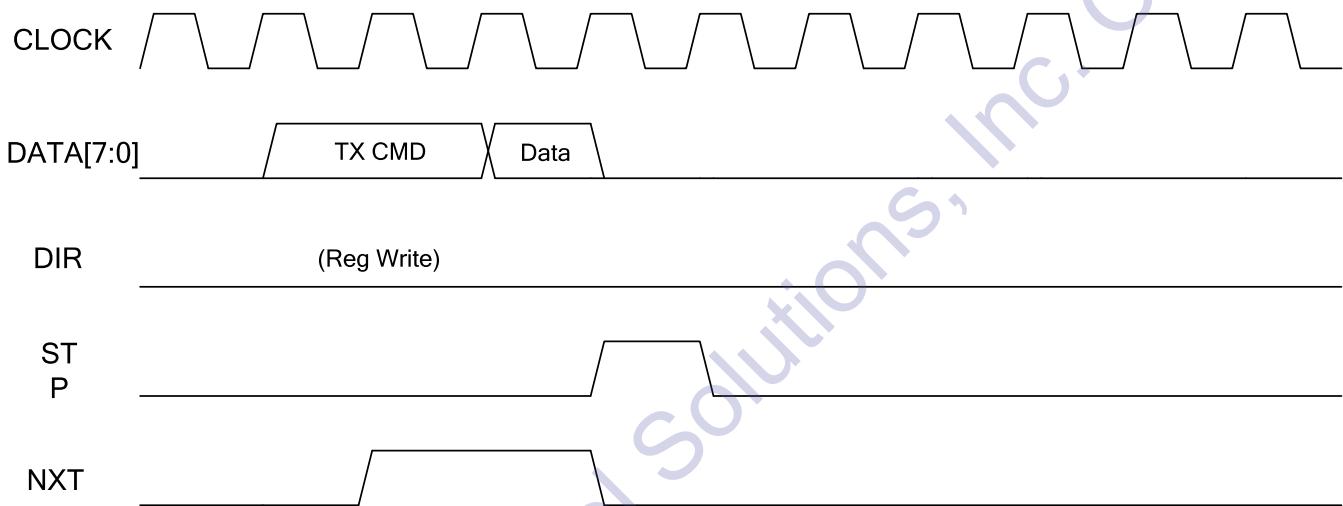


Figure 4. RegWrite Operation

For a register read, as shown in Figure 5, the Link sends a RegRead command and waits for NXT to assert. In the cycle after NXT asserts, the RN1133 asserts DIR to gain control of the bus. In the cycle after DIR asserts, the RN1133 returns the register read data. If the RN1133 aborts the RegRead by asserting DIR earlier, the Link must retry RegRead when the bus is idle.

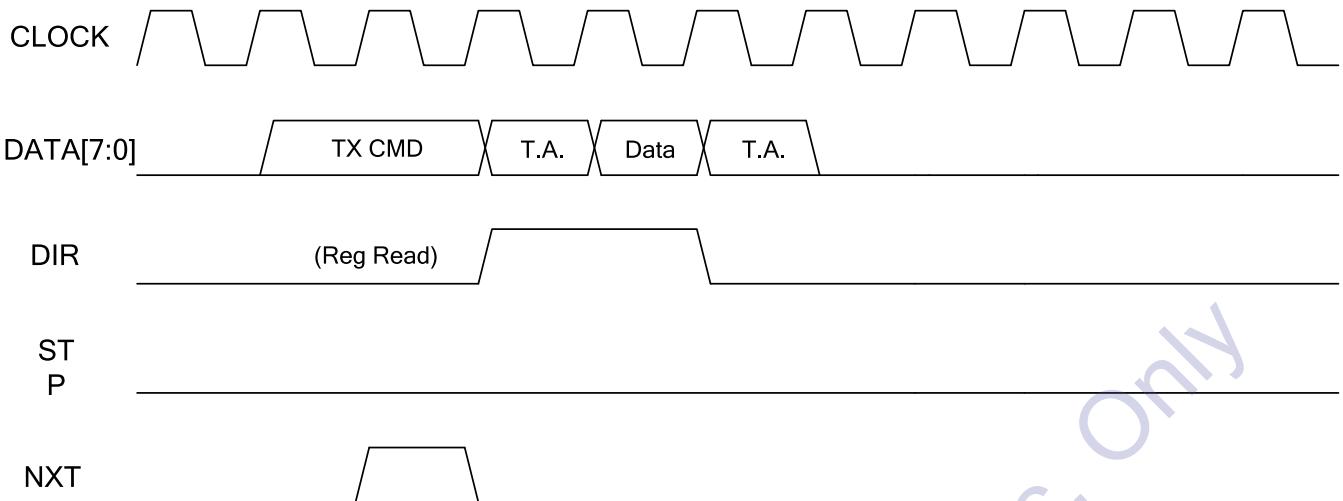


Figure 5. RegRead Operation

T.A. = Turn Around

To transmit USB packet data (as shown in Figure 6 and 7), the Link first drives a TX CMD and the RN1133 throttles the data using NXT such as the Link provides the next byte in the cycle after NXT is detected. When the last byte has been consumed by the RN1133, the Link asserted STP for one cycle, and drives DATA[7:0] to 00h if there's no transmit error. The Link must not assert STP before the first byte has been consumed by the RN1133.

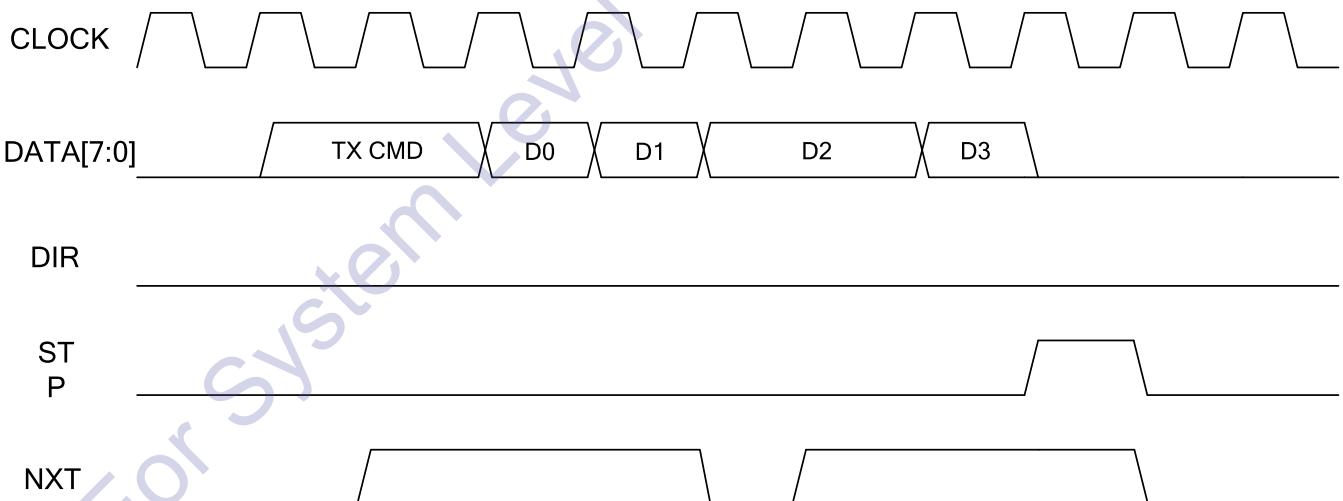


Figure 6. USB Packet Transmit in HS

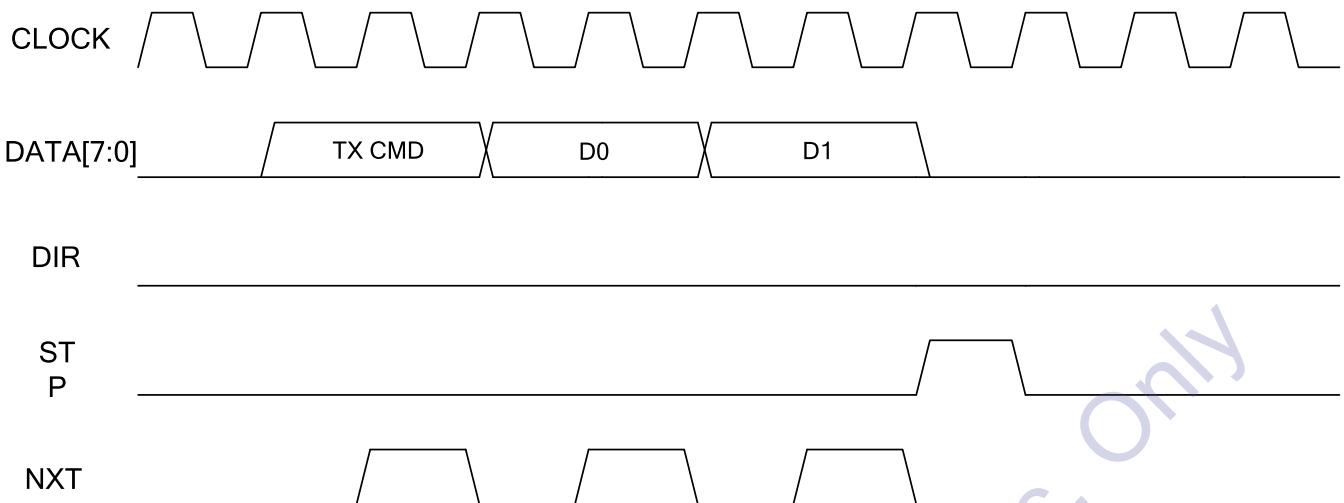


Figure 7. USB Packet Transmit in FS/LS

To receive USB packet data (as shown in Figure 8 and 9), the RN1133 gains data bus ownership by asserting DIR first. If DIR is previously low, the RN1133 will assert both DIR and NXT so that the Link knows immediately that this is an USB receive packet. If DIR is previously high, the RN1133 will de-assert NXT and drive a RX CMD with the RxEvent field set to 01b. The RN1133 will start driving data in the following cycle with an assertion of NXT, or will output RX CMD's with a de-assertion of NXT until USB data is available. All RX CMD changes will be signaled by the RN1133 when NXT is low. If NXT is never low during the USB packet receive, RN1133 will replace all RX CMD changes with a single RX CMD update at the end of USB packet receive.

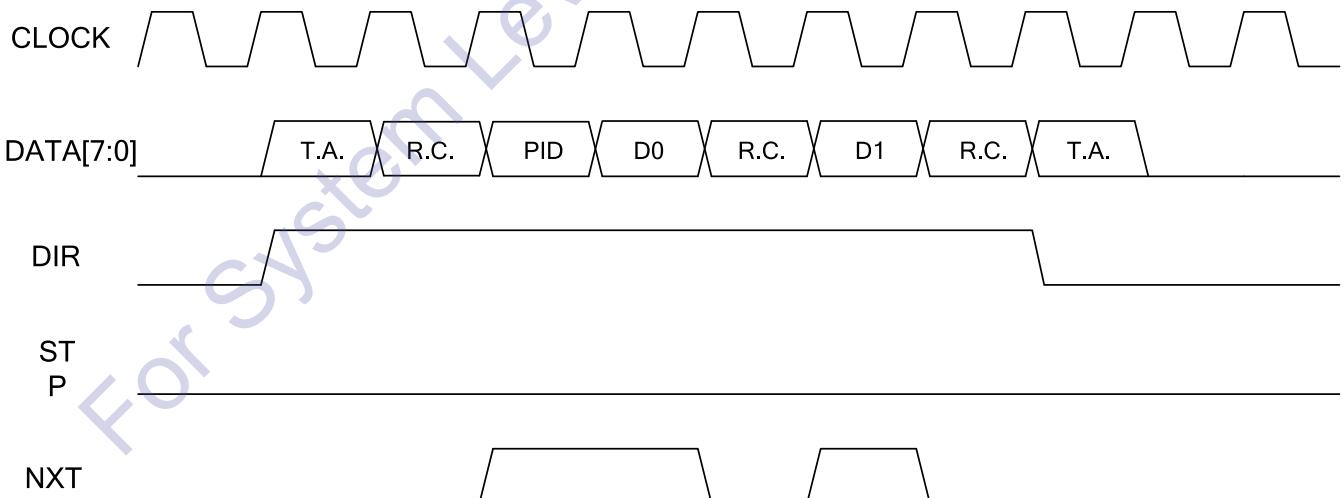


Figure 8. USB Packet Receive in HS

R.C. = RX CMD

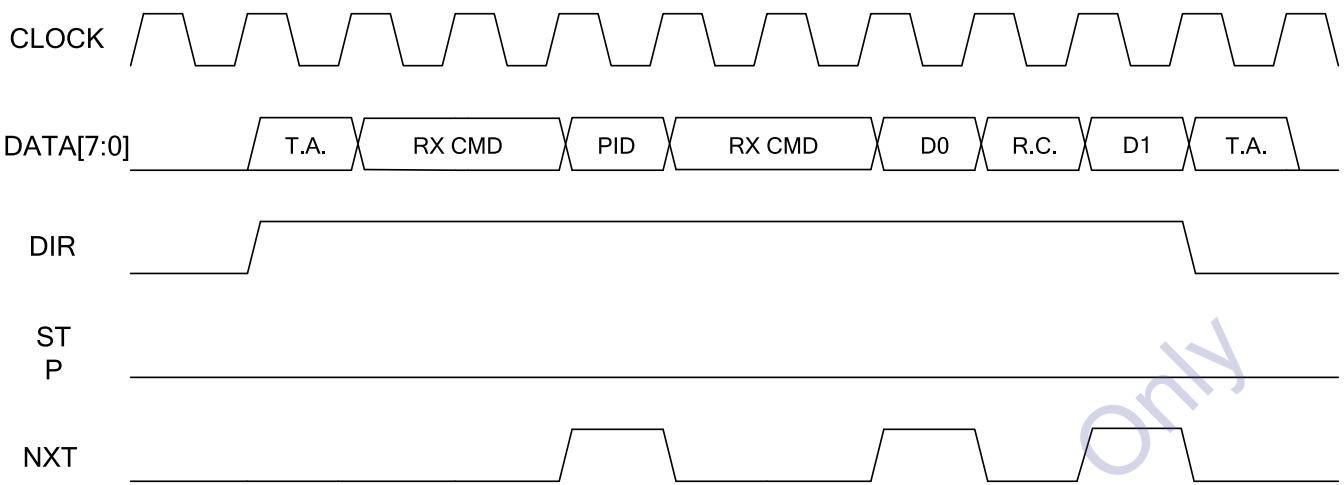


Figure 9. USB Packet Receive in FS/LS

R.C. = RX CMD

8.1.2 Low Power Mode

The Link can place the RN1133 into Low Power Mode when the USB bus is suspended. The RN1133 powers down most of the circuitry except the interface pins and full speed receiver. The 60MHz CLOCK is also stopped in this mode. When placed under the Low Power Mode, the RN1133 drives DATA[3:0] as defined in Table 6. LineState is driven via a combinational logic from the FS transceiver. The Int pin is asserted whenever any un-masked interrupt occurs.

Table 6. Low Power Mode Pin Definition

Signal	Maps to	Direction	Description
Linestate (0)	DATA[0]	OUT	Combinatorial LineState(0) driven directly by FS analog receiver
Linestate (1)	DATA[1]	OUT	Combinatorial LineState(1) driven directly by FS analog receiver
Reserved	DATA[2]	OUT	Reserved and driven to low
Int	DATA[3]	OUT	Active high interrupt indication

The Link sets SuspendM bit in the Function Control register to 0b to place RN1133 into Low Power Mode. While in Low Power Mode, the RN1133 asserts DIR and de-asserts NXT. The RN1133 starts driving the signals after the one clock turn around cycle. (Please refer to the following Figure 10)

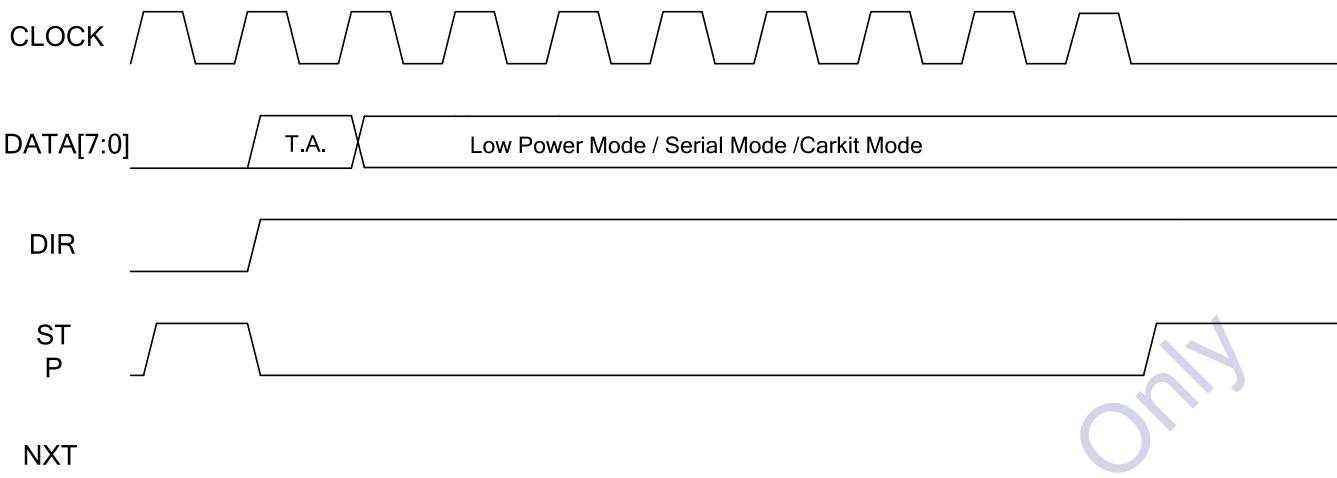


Figure 10. Enter Low Power Mode

T.A. = Turn Around

As shown in Figure 11, the Link can signal the RN1133 to exit Low Power Mode by asserting STP. The RN1133 starts to wake up and when the CLOCK signal meets ULPI timing requirements, the RN1133 de-asserts DIR. The SuspendM bit is also automatically set to 1b at this time. The Link has to de-assert STP to complete the operation. The RN1133 stops driving the Low Power Mode signals after one cycle of bus turnaround.

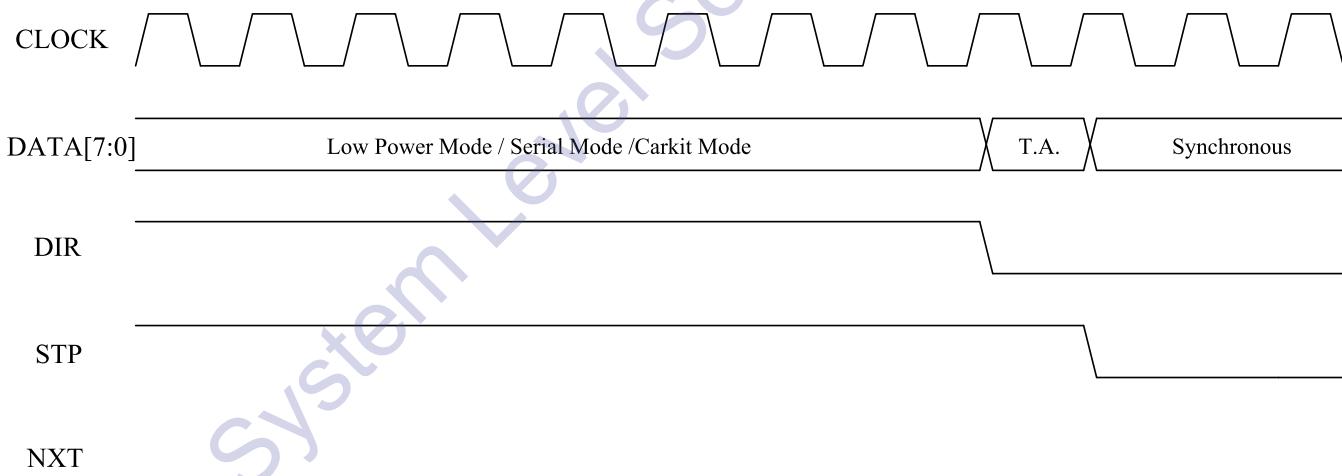


Figure 11. Exit Low Power Mode

T.A. = Turn Around

8.1.3 6-Pin FsLs Serial Mode

The Link can place the RN1133 into 6-Pin FsLs Serial Mode by setting the 6-Pin FsLsSerialMode bit in the Interface Control register, the RN1133 enters and exits the 6-Pin FsLS Serial Mode in the same manner as the Low Power Mode. Table 7 shows the pin definition of 6-Pin FsLs Serial Mode:

Table 7. 6-Pin FsLs Serial Mode Pin Definition

Signal	Maps to	Direction	Description
Tx_enable	DATA[0]	IN	Active high transmit enable
Tx_dat	DATA[1]	IN	Transmit differential data on D+/D-
Tx_se0	DATA[2]	IN	Transmit singled-ended zero on D+/D-
Int	DATA[3]	OUT	Active high interrupt indication.
Rx_dp	DATA[4]	OUT	Single-ended receive data from D+
Rx_dm	DATA[5]	OUT	Single-ended receive data from D-
Rx_rcv	DATA[6]	OUT	Differential receive data from D+/D-
Reserved	DATA[7]	OUT	Reserved. This pin is driven low by RN1133.

8.1.4 3-Pin FsLs Serial Mode

RN1133 also supports 3-Pin FsLs Serial Mode which can be enabled by the Link setting the 3-Pin FsLsSerialMode bit in the Interface Control register. RN1133 also enters and exits the 3-Pin FsLs Serial Mode in the same manner as in Low Power Mode. Table 8 shows the pin definition in 3-Pin FsLs Serial Mode:

Table 8. 3-Pin FsLs Serial Mode Pin Definition

Signal	Maps to	Direction	Description
Tx_enable	DATA[0]	IN	Active high transmit enable
Dat	DATA[1]	I/O	Transmit differential data on D+/D- when Tx_enable is high Receive differential data on D+/D- when Tx_enable is low
Se0	DATA[2]	I/O	Transmit singled-ended zero on D+/D- when Tx_enable is high Receive singled-ended zero on D+/D- when Tx_enable is low
Int	DATA[3]	OUT	Active high interrupt indication.

8.1.5 Carkit Mode

Carkit Mode is supported when the Link sets the CarkitMode bit the Interface Control register. The Carkit mode allows the Link to communicate through the RN1133 to a remote carkit using UART signaling. The RN1133 enters and exits Carkit mode in the same manner as the Low Power Mode. Table 9 shows the pin definition of Carkit Mode:

Table 9. Carkit Mode Pin Definition

Signal	Maps to	Direction	Description
Txd	DATA[0]	IN	UART TXD signal that is routed to D- pin.
Rxd	DATA[1]	OUT	UART RXD signal that is routed from D+ pin.
Reserved	DATA[2]	-	Reserved
Int	DATA[3]	OUT	Active high interrupt indication.

8.2 PLL and Crystal Oscillator

The RN1133's internal PLL and crystal oscillator circuits generate an accurate 480MHz clock to the USB Transceiver from the 24MHz clock input. Two modes of clock operations are allowed for greater flexibilities:

- (1) 24MHz external crystal: The crystal oscillator will generate a sine wave which feeds into PLL and serves as its reference clock. With this reference clock, PLL generates different clock frequencies to the system.
- (2) 24MHz clock generator: A 24MHz clock can be fed directly to pin XIN and XOUT to be left open at the same time. This clock source can also serve as the reference clock for PLL to generate different clock frequencies to the system.

Due to the architecture of USB protocol, a low-jitter clock is necessary to recover clock phase from data hence the input clock's frequency tolerance is recommended to be less than +/- 100 ppm to ensure the +/- 500ppm specification required by the USB specification.

8.3 Reference and Bias

The RN1133's internal bandgap reference circuit generates the absolute current and biasing for the analog circuit. An external 20K Ohm reference resistor is required to connect REXT pin to ground.

8.4 1.8V Voltage Regulator

The RN1133's integrated voltage regulator provides 1.8V output for the internal logic from the 3.3V input and the 1.8V output shall not be used to power any external chip. The voltage regulator guarantees +/- 5% accuracy output voltage with short circuit protection. A 0.1uF and a 4.7uF bypass capacitors are required for the VD18 pin. The integrated regulator can be enabled by connecting the VD18_EN pin to high (3.3V power) and be disabled by connecting the V18_EN pin to ground. External 1.8V power has to be supplied to the VD18 pin when the internal 1.8V voltage regulator is disabled and the 1.8V power can only be supplied after the 3.3V power has already been supplied.

8.5 Power On Reset

The RN1133's on chip power on reset circuit resets all logic and analog circuits after the 1.8V core voltage produced by the internal voltage regulator becomes stable. A recommended power on sequence is depicted in Figure 12 to power on the 3.3V power supply first then the 1.8V power supply to avoid latch up occurrences. Such sequence is guaranteed by enabling the internal voltage regulator which produces a 500 us start-up time delay for its 1.8V output to the 3.3V power supply. The RN1133's power on reset circuit also provides a tri-state mechanism which guarantees a correct USB initial state regardless of the unstable state during reset. As shown in Figure 12, these

steps in turn guarantee the system work in a proper way.

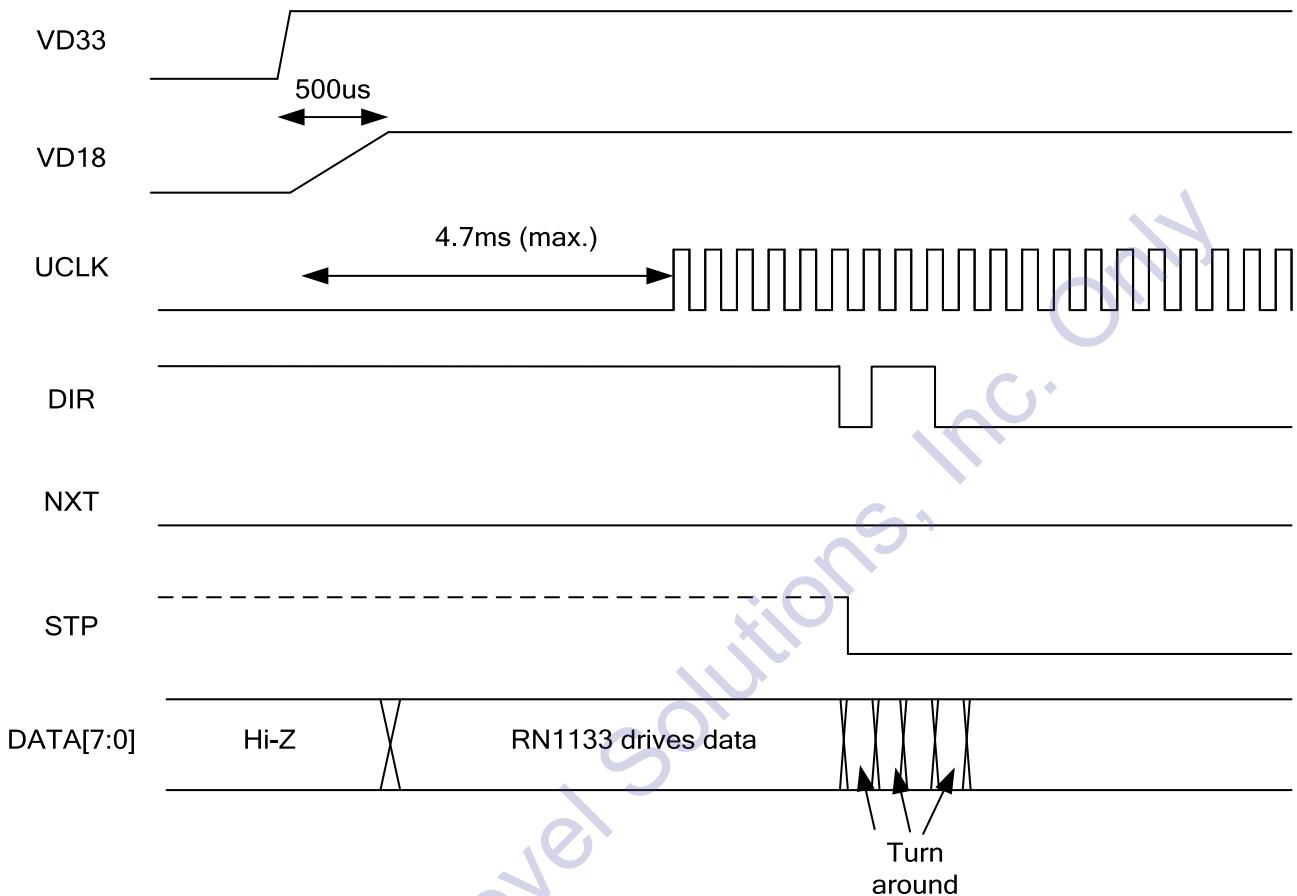


Figure 12. Power On Reset Sequence

8.6 OTG

The OTG circuit enables RN1133 to comply with the *On-The-Go Supplement to the USB 2.0 Specification*. The OTG circuit allows the RN1133 to be configured as a host or a peripheral depending on the type of cable being inserted to the connector. When a Micro-A cable is inserted, the RN1133 will be configured as a host (A-Device) and when a Micro-B cable is inserted, the RN1133 will be configured as a peripheral (B-Device). The OTG circuit consists of three parts: ID Detect, VBUS Comparator and SRP Discharge/Charge Resistor.

8.6.1 ID Detect

The ID Detect circuit together with the ID pin detects the type of cable being inserted. If a Micro-A cable is inserted,

the ID pin is shorted to ground. On the other hand, if a Micro-B cable is inserted, the ID pin is floated and its integrated pull-up resistor pulls the value to high (3.3V). The pull-up resistor can be disabled by the IdPullUp bit in the OTG Control register in order to save power. However, a weak pull-up resistor is still present to prevent a floating value for the ID pin. The IdGnd bit of the USB Interrupt Status Register shows whether the ID pin is connected to ground or not and it can be configured to generate an interrupt when required. Table 10 summarizes the ID pin detection combination:

Table 10. ID Pin Detection Combination

USB Cable Type	OTG Role	ID Voltage	IdGnd bit
Micro-A	Host (A-Device)	0	0
Micro-B	Peripheral (B-Device)	3.3V	1

8.6.2 VBUS Comparator

The VBUS Comparator ensures the VBUS Valid, Session Valid and Session End conditions are met as required by the *On-The-Go Supplement to the USB 2.0 Specification*. VBUS Valid condition is determined by the VBUS Comparator as the VBUS voltage to remain above 4.4V when the A-Device is configured to provide 8-100mA. For the A-Device to provide 100 to 500mA, an external VBUS comparator is required to ensure the VBUS voltage does not go below 4.75V. The external VBUS comparator is supported thru the VVE pin and it can be used by the RN1133 by enabling the UseExternalVbusIndicator bit of the OTG Control register. Session Valid detection is required when the RN1133 is configured as either an A-Device or B-Device. For the A-Device configuration, Session Valid detects Session Request Protocol (SRP). For the B-Device configuration, VBUS Valid detects the presence of VBUS. The RN1133 indicates the Session Valid status with the SessValid bit in the USB Interrupt Status register. Session End is determined when VBUS is less than 0.5V. Its status is indicated by the SessEnd bit of the USB Interrupt Status register.

8.7 USB Transceiver/CDR

The USB Transceiver/CDR consists of a HS/FS/LS transmitter, a HS/FS/LS receiver, a serial to parallel data converter and a clock data recovery circuit. The HS/FS/LS transmitter is responsible to transmit data directly onto the USB cable while the HS/FS/LS receiver is responsible to receive data directly from the USB cable. Both Squelch and SE0 detection circuits are integrated with the receiver. The serial to parallel data converter converts parallel data from the ULPI Interface to USB serial data format and vice versa while the clock recovery circuit derives a reference clock for the receiver. This module also integrates the 1.5K Ohm pull-up, 23K Ohm pull-down and 45 Ohm termination resistors for both DP, DM. Their valid combinations are determined by the registers in Table 27.

9. ULPI Registers

The RN1133 supports the Immediate Register Set defined in the ULPI Specification, Revision 1.1. Table 11 shows the RN1133's register definition in detail.

9.1 Register Map

Table 11 shows RN1133 register's 6-bit address which forms part of the **TX CMD Byte**.

Table 11. Register Table

Field Name	Size (bits)	Address (6 bits)			
		Rd	Wr	S	C
Vendor ID Low	8	00h	-	-	-
Vendor ID High	8	01h	-	-	-
Product ID Low	8	02h	-	-	-
Product ID High	8	03h	-	-	-
Function Control	8	04-06h	04h	05h	06h
Interface Control	8	07-09h	07h	08h	09h
OTG Control	8	0A-0Ch	0Ah	0Bh	0Ch
USB Interrupt Enable Rising	8	0D-0Fh	0Dh	0Eh	0Fh
USB Interrupt Enable Falling	8	10-12h	10h	11h	12h
USB Interrupt Status	8	13h	-	-	-
USB Interrupt Latch	8	14h	-	-	-
Debug	8	15h	-	-	-
Scratch	8	16-18h	16h	17h	18h
Carkit Control	8	19-1Bh	19h	1Ah	1Bh
Reserved	8	1Ch	-	-	-
Carkit Interrupt Enable	8	1Dh-1Fh	1Dh	1Eh	1Fh
Carkit Interrupt Status	8	20h	-	-	-
Carkit Interrupt Latch	8	21h	-	-	-
Reserved	8	22-3Fh			

Rd - Read: Register can be read. Read-only if this is the only mode given.

Wr - Write: Pattern on the data bus will be written over all bits of the register.

Set - Set: Pattern on the data bus is OR'd with and written into the register.

Clr - Clear: Pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

9.1.1 Vendor ID and Product ID

Address: 00h – 03h (Read)

VID/PID information

Table 12. VID/PID Register

Register	Bits	Access	Address	Description
Vendor ID Low	7:0	Rd	00h	Lower byte of RN1133's Vendor ID. 9Ch.
Vendor ID High	7:0	Rd	01h	Upper byte of RN1133's Vendor ID. 19h.
Product ID Low	7:0	Rd	02h	Lower byte of RN1133's Product ID. 00h.
Product ID High	7:0	Rd	03h	Upper byte of RN1133's Product ID. 04h.

9.1.2 Function Control

Address: 04h – 06h (Read), 04h(Write), 05h(Set), 06h(Clear)

Controls function setting of RN1133

Table 13. Function Control Register

Field name	Bits	Access	Reset	Description
XcvrSelect	1:0	Rd/Wr/S/C	01b	<p>Selects the required transceiver speed.</p> <p>00b : Enables HS transceiver</p> <p>01b : Enables FS transceiver</p> <p>10b : Enables LS transceiver</p> <p>11b : Enables FS transceiver for LS packets (FS preamble is automatically pre-pended)</p>
TermSelect	2	Rd/Wr/S/C	0b	<p>Controls the internal 1.5kΩ pull-up, 23K pull down resistors and 45Ω HS termination. Control over bus resistors changes depending on XcvrSelect, OpMode, and DpPulldown, DmPulldown of the OTG Control register. Please refer to Table 27 for their resultant combinations.</p>
OpMode	4:3	Rd/Wr/S/C	00b	<p>Selects the required bit encoding style during transmit.</p> <p>00b: Normal operation.</p> <p>01b: Non-driving.</p> <p>10b: Disable bit-stuff and NRZI encoding.</p> <p>11b: Reserved.</p>

Field name	Bits	Access	Reset	Description
Reset	5	Rd/Wr/S/C	0b	Active high transceiver reset. After the Link sets this bit, the RN1133 asserts DIR and resets its transceiver. When the reset is completed, the RN1133 de-asserts DIR and automatically clears this bit. After de-asserting DIR, the RN1133 re-asserts DIR and sends a RX CMD update to the Link. The Link must wait for DIR to de-assert before using the ULPI bus. This bit does not reset the ULPI interface and its register set.
SuspendM	6	Rd/Wr/S/C	1b	Active low suspend. Puts RN1133 into Low Power Mode. The RN1133 powers down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The RN1133 automatically sets this bit to '1' after exiting from Low Power Mode. 0b : Low Power Mode 1b : Powered
Reserved	7	-	0b	Reserved.

9.1.3 Interface Control

Address: 07h – 09h (Read), 07h(Write), 08h(Set), 09h(Clear)

Enables alternative interfaces and features for RN1133.

Table 14. Interface Control Register

Field name	Bits	Access	Reset	Description
6-pin FsLsSerialMode	0	Rd/Wr/S/C	0b	Configures the ULPI interface to 6-pin Serial Mode. The RN1133 automatically clears this bit when serial mode is exited. 0b : FS/LS packets are sent using parallel interface. 1b : FS/LS packets are sent 6-pin using serial interface.
3-pin FsLsSerialMode	1	Rd/Wr/S/C	0b	Configures the ULPI interface to 3-pin Serial Mode. The RN1133 automatically clears this bit when serial mode is exited. 0b : FS/LS packets are sent using parallel interface. 1b : FS/LS packets are sent using 3-pin serial interface.
Reserved	2	-	0b	Reserved

Field name	Bits	Access	Reset	Description
ClockSuspendM	3	Rd/Wr/S/C	0b	<p>Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry. Valid only when SuspendM = 1b. The RN1133 ignores ClockSuspend when SuspendM = 0b.</p> <p>By default, the clock will not be enabled in Serial Modes.</p> <p>0b : Clock will not be enabled in Serial Modes.</p> <p>1b : Clock will be enabled in Serial Modes.</p>
AutoResume	4	Rd/Wr/S/C	1b	Enables the RN1133 to automatically transmit resume signaling. Only applicable in the USB host mode.
Indicator Complement	5	Rd/Wr/S/C	0b	<p>Sets the RN1133 to invert the VVE input signal, generating the complement output.</p> <p>0b: RN1133 inverts VVE signal (default).</p> <p>1b: RN1133 does not invert VVE signal.</p>
Indicator PassThru	6	Rd/Wr/S/C	0b	<p>Controls whether the VVE complement output is qualified with the Internal VbusValid comparator before being used in the VBUS State in the RX CMD.</p> <p>0b: VVE complement output signal is qualified with the Internal VbusValid comparator.</p> <p>1b: VVE complement output signal is not qualified with the Internal VbusValid comparator.</p>
Interface Protect Disable	7	Rd/Wr/S/C	0b	<p>Controls circuitry for protecting the ULPI interface when the Link tri-states STP and DATA.</p> <p>0b: Enables the interface protect circuit (default).</p> <p>1b: Disables the interface protect circuit.</p>

9.1.4 OTG Control

Address: 0Ah – 0Ch (Read), 0Ah(Write), 0Bh(Set), 0Ch(Clear)

Controls OTG functions of RN1133.

Table 15. OTG Control Register

Field name	Bits	Access	Reset	Description
IdPullup	0	Rd/Wr/S/C	0b	Connects a pull-up to the ID line. 0b : Disables the pull-up of ID line. 1b : Enables the pull-up of ID line.
DpPulldown	1	Rd/Wr/S/C	1b	Connects the 15k Ohm pull-down resistor on D+ . 0b : Pull-down resistor not connected to D+ . 1b : Pull-down resistor connected to D+ .
DmPulldown	2	Rd/Wr/S/C	1b	Connects the 15k Ohm pull-down resistor on D- . 0b : Pull-down resistor not connected to D- . 1b : Pull-down resistor connected to D- .
DischrgVbus	3	Rd/Wr/S/C	0b	Discharges VBUS through a resistor. When the Link sets this bit to 1, it waits for a RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge. 0b : does not discharge VBUS 1b : discharges VBUS
ChrgVbus	4	Rd/Wr/S/C	0b	Charges VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first checks that VBUS has been discharged (via DischrgVbus bit), and that both D+ and D- data lines have been low (SE0) for 2ms. 0b : does not charge VBUS 1b : charges VBUS
DrvVbus	5	Rd/Wr/S/C	0b	Signals the external power supply to drive 5V on VBUS. 0b : does not drive VBUS (default) 1b : drives 5V on VBUS

Field name	Bits	Access	Reset	Description
DrvVbus External	6	Rd/Wr/S/C	0b	Selects between the internal and the external 5V Vbus supply. The bit is ORed with DrvVbus for better compatibilities. 0b: Does not drive VBUS using external power supply 1b : Drives VBUS using external power supply.
UseExternal VbusIndicator	7	Rd/Wr/S/C	0b	Tells the RN1133 to use an external VBUS valid indicator. 0b: Uses the internal VBUS comparator (default). 1b: Uses external VBUS valid indicator signal

9.1.5 USB Interrupt Enable Rising

Address: 0Dh – 0Fh (Read), 0Dh(Write), 0Eh(Set), 0Fh(Clear)

When set, the bits in this register cause an interrupt event notification to the Link when RN1133's signal changes from low to high. All transitions are enabled by default. To ensure interrupts are detectable when CLOCK is powered down, the Link should enable both rising and falling edges.

Table 16. USB Interrupt Enable Rising Register

Field name	Bits	Access	Reset	Description
Hostdisconnect Rise	0	Rd/Wr/S/C	1b	Generates an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode.
VbusValid Rise	1	Rd/Wr/S/C	1b	Generates an interrupt event notification when VbusValid changes from low to high.
SessValid Rise	2	Rd/Wr/S/C	1b	Generates an interrupt event notification when SessValid changes from low to high.
SessEnd Rise	3	Rd/Wr/S/C	1b	Generates an interrupt event notification when SessEnd changes from low to high.
IdGnd Rise	4	Rd/Wr/S/C	1b	Generates an interrupt event notification when IdGnd changes from low to high.
Reserved	7:5	-	000b	Reserved.

9.1.6 USB Interrupt Enable Falling

Address: 10h – 12h (Read), 10h(Write), 11h(Set), 12h(Clear)

When set, the bits in this register cause an interrupt event notification to the Link when RN1133's signal changes from high to low. All transitions are enabled by default. To ensure interrupts are detectable when CLOCK is powered down, the Link should enable both rising and falling edges.

Table 17. USB Interrupt Enable Falling Register

Field name	Bits	Access	Reset	Description
Hostdisconnect Fall	0	Rd/Wr/S/C	1b	Generates an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode.
VbusValid Fall	1	Rd/Wr/S/C	1b	Generates an interrupt event notification when VbusValid changes from high to low.
SessValid Fall	2	Rd/Wr/S/C	1b	Generates an interrupt event notification when SessValid changes from high to low.
SessEnd Fall	3	Rd/Wr/S/C	1b	Generates an interrupt event notification when SessEnd changes from high to low.
IdGnd Fall	4	Rd/Wr/S/C	1b	Generate an interrupt event notification when IdGnd changes from high to low.
Reserved	7:5	-	000b	Reserved.

9.1.7 USB Interrupt Status

Address: 13h (Read only)

This register indicates the current value of interrupt source signal.

Table 18. USB Interrupt Status Register

Field name	Bits	Access	Reset	Description
Hostdisconnect	0	Rd	0b	Current value of Hostdisconnect output. Applicable only in host mode. Automatically resets to 0b when Low Power Mode is entered.
VbusValid	1	Rd	0b	Current value of VbusValid output.
SessValid	2	Rd	0b	Current value of SessValid output.
SessEnd	3	Rd	0b	Current value of SessEnd output.

Field name	Bits	Access	Reset	Description
IdGnd	4	Rd	0b	Current value of IdGnd output.
Reserved	7:5	-	000b	Reserved.

9.1.8 USB Interrupt Latch

Address: 14h (Read only with auto clear)

The RN1133 sets these bits when an unmasked change occurs on the corresponding signal. The RN1133 will automatically clear all bits when the Link reads this register, or when Low Power Mode, Serial Mode or Carkit Mode is entered.

Table 19. USB Interrupt Latch Register

Field name	Bits	Access	Reset	Description
Hostdisconnect Latch	0	Rd	0b	Sets to 1b when an unmasked event occurs on Hostdisconnect . Cleared when this register is read. Applicable only in host mode.
VbusValid Latch	1	Rd	0b	Sets to 1b when an unmasked event occurs on VbusValid . Cleared when this register is read.
SessValid Latch	2	Rd	0b	Sets to 1b when an unmasked event occurs on SessValid . Cleared when this register is read.
SessEnd Latch	3	Rd	0b	Sets to 1b when an unmasked event occurs on SessEnd . Cleared when this register is read.
IdGnd Latch	4	Rd	0b	Sets to 1b when an unmasked event occurs on IdGnd . Cleared when this register is read.
Reserved	7:5	-	000b	Reserved.

Table 20 shows the rule for RN1133 to set its interrupt latch register bits. If register read data is returned to the Link in the same cycle that an USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set.

Table 20. USB Interrupt Latch Register Rule

Input Conditions		Resultant value of USB Latch Register bit
Register read data returned in current clock cycle	USB Interrupt Latch bit to be set in current clock cycle	
No	No	0
No	Yes	1
Yes	No	0
Yes	Yes	0

9.1.9 Debug

Address: 15h (Read only)

This register shows the current values of Linestate[1:0] for debugging.

Table 21. Debug Register

Field name	Bits	Access	Reset	Description
LineState0	0	Rd	0b	Contains the current value of LineState(0)
LineState1	1	Rd	0b	Contains the current value of LineState(1)
Reserved	7:2	-	000000b	Reserved.

9.1.10 Scratch

Address: 16h-18h (Read), 16h(Write), 17h(Set), 18h(Clear)

An empty register for the Link to test read, write, set and clear operations.

Table 22. Scratch Register

Field name	Bits	Access	Reset	Description
Scratch	7:0	Rd/Wr/S/C	00h	Empty register byte for testing purposes. The Link can read, write, set, and clear this register and the RN1133's functionality will not be affected.

9.1.11 Carkit Control

Address: 19h-1Bh (Read), 19h(Write), 1Ah(Set), 1Bh(Clear)

This register controls the carkit circuitry of RN1133 in conjunction with the **CarkitMode** bit in the Interface Control register. If the **CarkitMode** bit is not set, **Carkitpwr**, **TxdEn** and **RxdEn** bits are ignored. If the **CarkitMode** bit is set but the **RxdEn** bit is not set, then the DATA[1] becomes logic high.

Table 23. Carkit Control Register

Field name	Bits	Access	Reset	Description
CarkitPwr	0	Rd/Wr/S/C	0b	Applies power to carkit circuitry.
IdGndDrv	1	Rd/Wr/S/C	0b	Drives ID pin to ground.
TxdEn	2	Rd/Wr/S/C	0b	Routes TXD signal from DATA(0) pin to D- pin.
RxdEn	3	Rd/Wr/S/C	0b	Routes RXD signal from D+ pin to DATA(1) pin.
Reserved	7:4	-	0000b	Reserved.

9.1.12 Carkit Interrupt Enable

Address: 1Dh-1Fh(Read), 1Dh(Write), 1Eh(Set), 1Fh(Clear).

When set, the bits in this register cause an interrupt event notification to be generated to the Link when the corresponding RN1133's signal changes.

Table 24. Carkit Interrupt Enable Register

Field name	Bits	Access	Reset	Description
IdFloat Rise	0	Rd/Wr/S/C	0b	Generates an interrupt to the Link when the ID pin changes from not floating to floating. The IdPullup bit in the OTG Control register must be set at this time.
IdFloat Fall	1	Rd/Wr/S/C	0b	Generates an interrupt to the Link when the ID pin changes from floating to not floating. The IdPullup bit in the OTG Control register must be set at this time.
Reserved	7:2	-	000000b	Reserved.

9.1.13 Carkit Interrupt Status

Address: 20h(Read only).

This register indicates which event triggered the carkit interrupt to the Link.

Table 25. Carkit Interrupt Status Register

Field name	Bits	Access	Reset	Description
IdFloat	0	Rd	0b	Asserted when the ID pin is floating.
Reserved	7:1	-	0000000b	Reserved.

9.1.14 Carkit Interrupt Latch

Address: 21h(Read only with auto clear).

The RN1133 sets these bits when an unmasked carkit event occurs. The RN1133 automatically clears all bits when the Link reads this register or when the Low Power Mode is entered. The rule of USB Interrupt Latch register table also applies to this register.

Table 26. Carkit Interrupt Latch Register

Field name	Bits	Access	Reset	Description
IdFloat Latch	0	Rd	0b	Asserted when the ID signal changes from not floating to floating if the IdFloat Rise bit in the Carkit Interrupt Enable register is set. Also asserted when the ID signal changes from floating to not floating if the IdFloat Fall bit in the Carkit Interrupt Enable register is set.
Reserved	7:1	-	0000000b	Reserved.

9.1.15 Reserved

Address: 22h-3Fh .

These registers are reserved.

9.2 Register Settings for All Upstream and Downstream Signaling Modes

Table 27 shows the register settings applied by the Link for the desired signaling mode. The RN1133 will generate the correct signaling, append the SYNC and EOP automatically as required. Table 27 also shows which resistors are enabled as a result of the register settings.

- **rpu_dp_en** enables the $1.5\text{k}\Omega$ pull-up resistor on D+
- **rpu_dm_en** enables the $1.5\text{k}\Omega$ pull-up resistor on D-
- **rpd_dp_en** enables the $23\text{k}\Omega$ pull-down resistor on D+
- **rpd_dm_en** enables the $23\text{k}\Omega$ pull-down resistor on D-
- **hsterm_en** enables the 45Ω termination resistors on D+ and D-

Table 27. Register Setting for All Signaling Mode

Signaling Mode	Register Settings					Resistor Settings				
	XcvrSelect	TermSelect	OpMode	DpPullup	DmPullup	rpu_dp_en	rpu_dm_en	rpd_dp_en	rpd_dm_en	hsterm_en
General Settings										
Tristate Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or Vbus < Vth(SessEnd)	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host Hi-Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b

Signaling Mode	Register Settings					Register Settings				
	XcvrSelect	TermSelect	OpMode	DpPulldown	DmPulldown	rpu_dp_en	rpu_dm_en	rpd_dp_en	rpd_dm_en	hstmr_en
Host Settings										
Host Low Speed Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test_J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral Hi-Speed	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral Full Speed	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral Low Speed	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral Low Speed Suspend	10b	1b	00b	0b	0b	0b	1b	0b	0b	0b
Peripheral Low Speed Resume	10b	1b	10b	0b	0b	0b	1b	0b	0b	0b
Peripheral Test_J/Test_K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Hi-Speed	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG device, Peripheral Full Speed	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG device, Peripheral Test_J/Test_K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b

10. Electrical Characteristics

Table 28. Electrical Characteristics

Typical values are at VDA3 = 3.3V; VDD3 = 3.3V; Temp = 27 ° C; unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VDA3 USB domain current consumption						
HS transmit current	I33a(hs_t)	High speed continuous data transmit at 480MHz		29	35	mA
HS receive current	I33a(hs_r)	High speed continuous data receive at 480MHz		26	30	mA
FS operation current	I33a(fs)	Full speed continuous data transmit at 12MHz		15	18	mA
LS operation current	I33a(ls)	Low speed continuous data transmit at 1.5MHz		16	19	mA
Un-configured current	I33a(uncfg)	Bus idle, no USB activity		14		mA
All power down	I33a(pd)	Low power mode, OTG compator disabled		83		uA
Suspend current	I33a(spnd)	Low power mode		150		uA
VDD3 ULPI domain current consumption						
Un-configured current	I33d(uncfg)	Bus idle, no USB activity		7		mA
HS operation current	I33d(hs)	High speed continuous data transmit at 480MHz		7		mA
Suspend current	I33d(spnd)	Low power mode		90		uA
Input level of HS						
Squelch level	Vhssq			160		mV
Disconnect level	Vhsdsc		525	540	625	mV
Input level of FS						
Diff. input sensitivity	Vdi		200			mV
Diff. common mode range	Vcm		0.8		2.5	V
Output level of FS/LS						
Low	Vfsol	Pull up on DP, RL = 1.5K Ohm to 3.3V			0.3	V
High (Driven)	Vfsoh	Pull up on DP, DM, RL = 15K Ohm to GND	2.7	3.3	3.6	V
Output signal cross point	Vcsr		1.3		2.0	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output level of HS						
HS idle level	Vhs0i		-10		10	mV
HS data signal high	Vhs0h		360		440	mV
HS data signal low	Vhs0l		-10		-10	mV
Chirp J	Vchirppj		700		1100	mV
Chirp K	Vchirppk		-900		-500	mV
HS transmitter characteristic						
Rise time	Thsr	Drive 45K Ohm to GND on DP and DM	500			ps
Fall time	Thsf	Drive 45K Ohm to GND on DP and DM	500			ps
Driver output resistance	Zhsdrv		40.5		49.5	Ohm
HS data rate	Thsdrat		479.76	480	480.24	MHz
FS transmitter characteristic						
Rise time	Tfr	CL = 50pF, 10% to 90% of Voh – Vol	4		20	ns
Fall time	Tff	CL = 50pF, 10% to 90% of Voh – Vol	4		20	ns
Differential Rise and Fall time matching (Tr/Tf)	Tfrfm	CL = 50pF	90		111.1	%
LS transmitter characteristic						
Rise time	Tlr	CL = 200pF to 600pF	75		300	ns
Fall time	Tlf	CL = 200pF to 600pF	75		300	ns
Differential Rise and Fall time matching (Tr/Tf)	Tlrfm	CL = 200pF to 600pF	80		125	%
IO characteristic						
High level input voltage	Vih		2.0			V
Low level input voltage	Vil				0.8	V
High level output voltage	Voh		2.4			V
Low level output voltage	Vol				0.4	V
High level output current	Ioh	When Voh = 2.4V	8			mA
Low level output current	Iol	When Vol = 0.4V	8			mA
Input leakage current	II		-10		+10	uA
Pin capacitance	Cp				5	pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OTG detector circuit characteristic						
Sess_end	Vb_sess_end		0.2		0.8	V
A_valid	Va_sess_vld		0.8		2	V
Vbus_valid	Va_vbus_vld		4.4			V
IdGnd threshold	Va_idgnd_thr			0.15*VDA3		V

11. Absolute Maximum Ratings

Table 29. Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input/Output Supply Voltage	Vcc(I/O)	VD33A, VD33D	-0.5		3.6	V
		VD18	-0.5		2	V
Input Voltage	Vi	VBUS,VVE	-0.5		5.5	V
		DATA[0-7], NXT STP, CLOCK, DIR, XIN, XOUT, REXT, ID, DP, DM	-0.5		3.6	V
Storage Temperature Range	Tstg		-40		125	°C
Electrostatic Discharge Voltage	VESD	Human Body Model (HBM)				
		DP, DM, ID	+/-8K			V
		Other pins	+/-2K			V
Latch Up Current	Ilu		150			mA

12. Recommended Operating Conditions

Table 30. Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input/Output Supply Voltage	Vcc(I/O)	VD33A, VD33D	3.0	3.3	3.6	V
		VD18	1.62	1.8	1.98	V
Input Voltage	Vi	VBUS, VVE	0		5.25	V
		DATA[0-7],NXT, STP, CLOCK, DIR,XIN, XOUT, REXT, ID, DP, DM	0		3.6	V
Ambient Temperature Range	Tamb		-40	25	85	°C

13. Typical Application Diagram

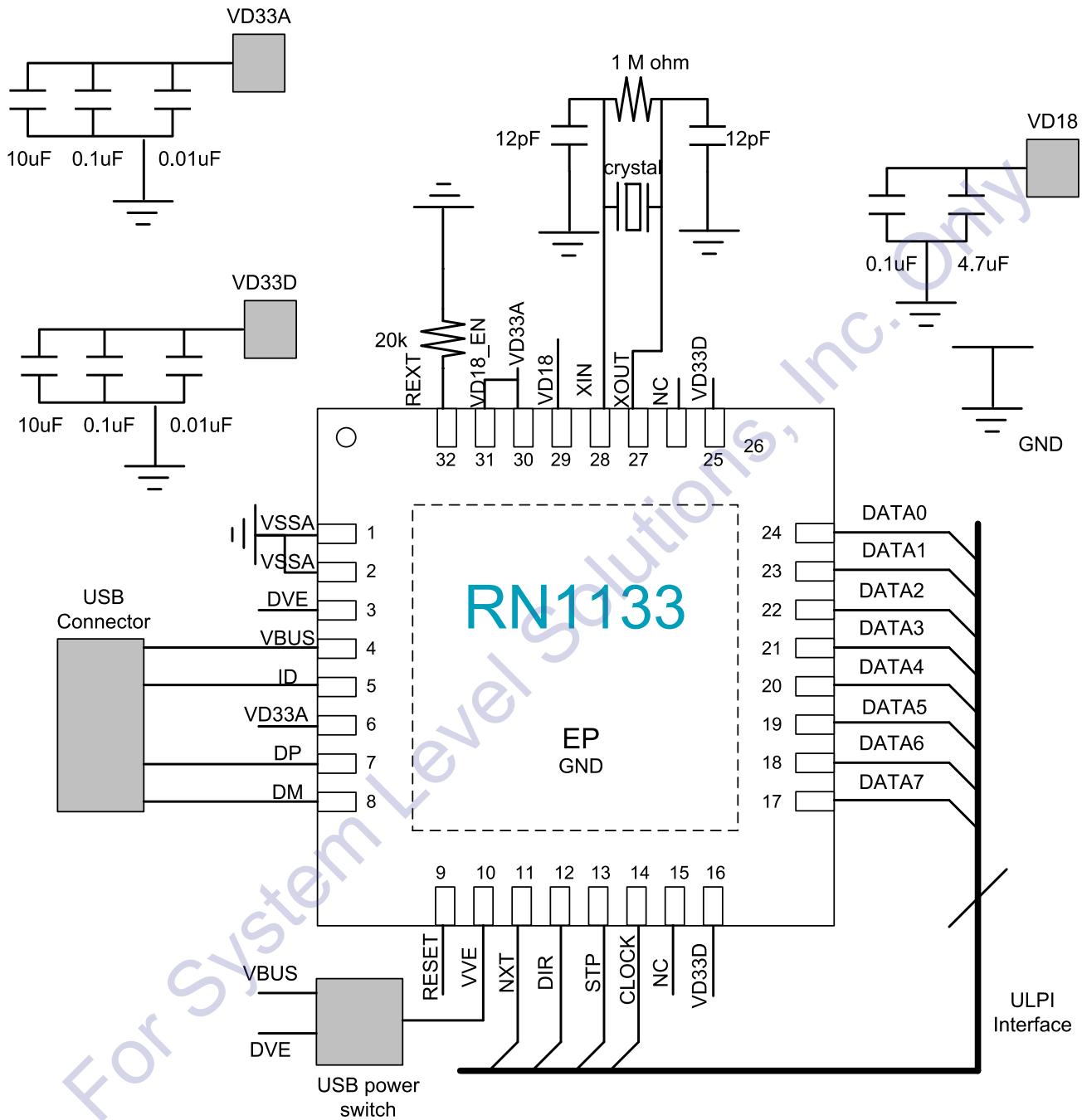
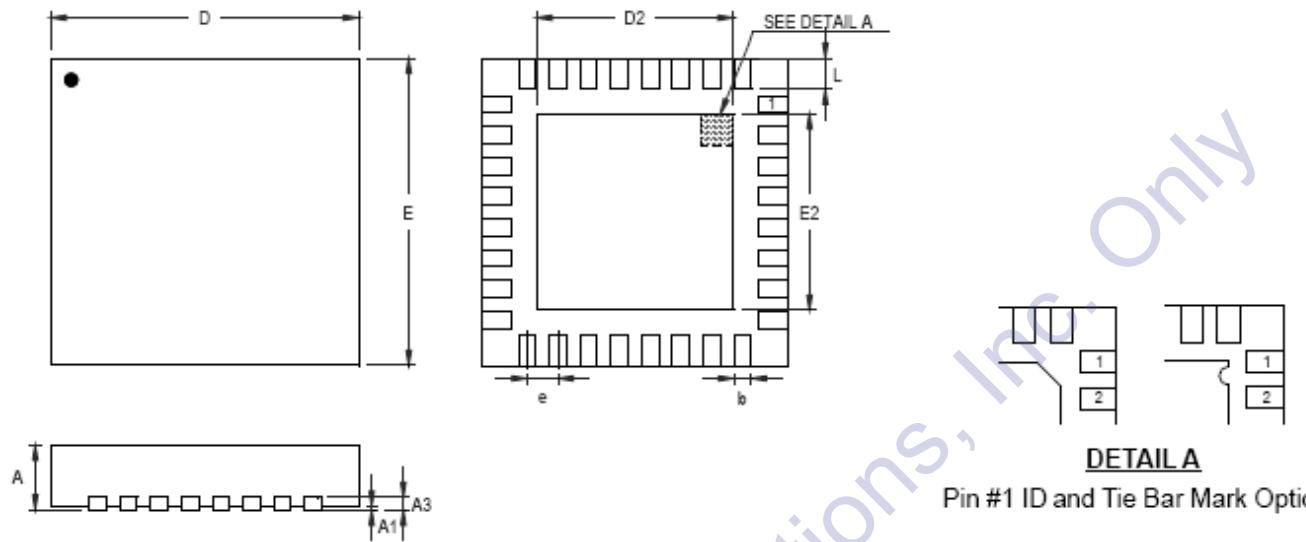


Figure 13. Typical Application Diagram

14. Package Outline



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

Figure 14. Package Outline

15. Datasheet Revision History

Table 31. Datasheet Revision History

VERSION	DATE	PAGE NO.	ITEM	DESCRIPTION
0.1	2007/8/22			Conceptual datasheet
0.9	2007/11/19	1-4, 8-32	Appended Ordering information, Table of Contents, Function Descriptions, ULPI Registers, Electrical Characteristics	Preliminary datasheet
0.91	2008/3/13	19, 37	Fig. 8.5 typo correction, Fig. 14 package outline update	Preliminary datasheet
0.92	2008/3/17	16, 22, 33	Table 8.1.3/8.1/4/8.1.5 bracket corrections, Table 9.1.2 opmode correction, Table 11 value correction	Preliminary datasheet
0.93	2008/4/30	1-40	Typo corrections, table title placement adjustments, table/figure designation corrections	Preliminary datasheet

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