SLS Multiple USB Solutions on a Single Chip using MAX10FPGA

Quick Start Guide

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Introduction

This document describes the steps for evaluating reference design of Multiple USB Solutions on a Single Chip using MAX10FPGA.

Table below shows the revision history of this document.

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
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<tbody>
<tr>
<td>1.1</td>
<td>June 2015</td>
<td>Updated steps and figures for USB to I2C Bridge and USB based ADC Interface</td>
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<tr>
<td>1.0</td>
<td>April 2015</td>
<td>First release</td>
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How to Contact SLS

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<table>
<thead>
<tr>
<th>Information Type</th>
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<tr>
<td>Product literature services, SLS literature services, Non-technical customer services, Technical support.</td>
<td><a href="mailto:support@slscorp.com">support@slscorp.com</a></td>
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## Typographic Conventions

The document uses the typographic conventions shown as below.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
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<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>All Headings and Sub Headings Titles in a document are displayed in bold type with initial capital letters; Example: <strong>Introduction</strong></td>
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<tr>
<td><strong>Bold Type with Italic Letters</strong></td>
<td>All Definitions, Figure and Table Headings are displayed in Italics. Examples: <strong>Figure 1. USB to I2C Bridge</strong></td>
</tr>
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<td><strong>1. 2.</strong></td>
<td>Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.</td>
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<td>•</td>
<td>Bullets are used in a list of items when the sequence of items is not important.</td>
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<tr>
<td><img src="hand_icon.png" alt="hand" /></td>
<td>The hand points to information that requires special attention.</td>
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<tr>
<td><img src="caution_icon.png" alt="caution" /></td>
<td>The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.</td>
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<tr>
<td><img src="warning_icon.png" alt="warning" /></td>
<td>The warning indicates information that should be read prior to starting or continuing the procedure or processes.</td>
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<tr>
<td><img src="feet_icon.png" alt="feet" /></td>
<td>The feet direct you to more information on a particular topic.</td>
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This document explains the steps for evaluating reference design of USB based bridges listed below.

- USB to I2C Bridge
- USB based ADC Interface
- USB to UART Bridge

Hardware Requirements for evaluating the reference design:

- Altera MAX 10 FPGA Evaluation Kit
- SLS MAX 10 Evaluation Kit Add On board
- USB mini cable (For Device Connection and as a Power Cable)
- USB Blaster
- For USB to UART Bridge, you may require the other UART Hardware for testing purpose

Please contact us for evaluation License regarding SLS IP Cores.

Below section describes the details of individual USB bridge and steps for testing on MAX10 Evaluation Kit Add on board.

**USB to I2C Bridge**

Aim of this bridge is to access I2C slave Device using an USB Interface. On the MAX10 Evaluation Kit Add On Board, we have AT24C01C PROM with I2C interface. In order to access this device, SLS has develop a Host application which will read and write the PROM using USB interface. As shown in Figure 1., this design uses the SLS USB 2.0 Device IP Core and I2C Master IP Core to communicate with the I2C Slave device and the Host machine.
Follow the steps to test USB to I2C Bridge using SLS Host Application.

1. Connect the MAX 10 Evaluation Kit Add On Board on MAX 10 Evaluation Kit.
2. Connect the USB Blaster to the board.
3. Power ON the board.
4. Go to `<MAX10 EV Kit AOB Installation Path>/hardware/demo/i2c_adc_intf_max10ev` folder.
5. Double click on `i2c_adc_intf_max10ev.bat` file. This will program SOF file on the board. You will see the message as shown in Figure 2.
6. After successful downloading USB 2.0 device detected in the Host machine. Install USB 2.0 device driver from `<MAX10 EV Kit AOB Installation Path>/software/driver` folder.

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**Figure 1. USB to I2C Bridge**

![USB to I2C Bridge Diagram](image-url)
7. Open Host Interface utility available in `<MAX10 EV Kit AOB Installation Path>/software/utility` folder. Figure 3 shows the MAX10 Evaluation Kit Add On Board Interface Utility.

8. To read any page from I2C Slave PROM device, enter page number and press “Read” button. Read data will be displayed on Utility.

9. To write any page to I2C Slave PROM device, enter page number, data (8 bytes) and press “Write” button.
USB based ADC Interface

Aim of this design is to provide the ADC interface over USB interface. The MAX10 Evaluation Kit Add On Board is having Analog GPIO headers which is directly connected to Altera MAX10 FPGA. As shown in Figure 4, this design uses the SLS USB 2.0 Device IP Core and Altera's ADC interface IP Core. On successful enumeration, the MAX10 Evaluation Kit Add On Board interface utility provides the option to select ADC channels to display the analog input signals.
Follow the steps to read ADC channels.

1. Connect the MAX 10 Evaluation Kit Add On Board on MAX 10 Evaluation Kit.
2. Connect the USB Blaster to the board.
3. Power ON the board.
4. Go to `<MAX10 EV Kit AOB Installation Path>/hardware/demo/i2c_adc_intf_max10ev` folder.
5. Double click on `i2c_adc_intf_max10ev.bat` file. This will program SOF file on the board. You will see the message as shown in Figure 5.
6. After successful downloading USB 2.0 device detected in the Host machine. Install USB 2.0 device driver from `<MAX10 EV Kit AOB Installation Path>/software/driver` folder.

7. After successful enumeration of USB 2.0 device, open the Host interface application from `<MAX10 EV Kit AOB Installation Path>/software/utilities` folder.

8. Go to ADC Channel Read tab. Figure 6. shows the screen shot of the MAX10 Evaluation Kit Add On Board interface utility for ADC interface.

9. Select the channels as per analog signal input and press “Start” button. User can observe graph of selected channels.

10. User can stop the conversion by pressing “Stop” button.
Figure 6. MAX10 Evaluation Kit Add On Board Interface Utility for ADC Interface