USB 2.0 OTG Transceiver with ULPI Interface

1. General Description

The RN1133 is a high performance USB 2.0 transceiver chip which supports low speed (LS), full speed (FS) and high speed (HS) data rates. The interface to a link controller is via the UTMI+ Low Pin Interface (ULPI). RN1133 also supports the on-the-go (OTG) mode which allows both Host and Peripheral operations. An up to 8KV HBM ESD protection circuit is integrated to the USB connection pins providing stronger ESD protection while reducing BOM at the same time. With the built-in 3.3V to 1.8V regulator and power on reset circuit, RN1133 is the best choice in terms of both performance and cost for USB 2.0 OTG transceiver applications.

2. Ordering Information

RN1133 ☐ ☐

- Package Type
  - QW : WQFN-32L 5x5 (W-Type)
- Operating Temperature Range
  - E : Pb Free with Industrial Standard
  - G: Green (Halogen Free with Commercial Standard)

Note :

Richnex Pb-free and Green products are:

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

3. Features

- **Complies with *Universal Serial Bus Specification Rev. 2.0.***
- **USB-IF OTG Compliance Test certified. TID: 100000021.**
- **Compatible with *USB On-The-Go Supplement Rev. 1.3.***
- **Complies with *UTMI+ Low Pin Interface (ULPI) Rev. 1.1.***
- **Complies with ULPI 8 bit mode.**
- **Supports ULPI 3/6 bit serial interface modes.**
- **Supports the USB Host Negotiation Protocol (HNP) and Session Control Protocol (SRP).**
- **Supports USB FS pre-amble packets.**
- **Supports Carkit Mode which routes UART signals thru USB pins.**
- **Integrated 24MHz crystal oscillator allows both crystal and input clock operations.**
- **Only requires a single 3.3V power supply with an integrated 3.3V to 1.8V LDO.**
- **+/- 8kV ESD protection on DP, DM and ID pins.**
- **Integrated Power On Reset circuit.**
- **Low power consumption and suspend current for portable applications.**
- **Small footprint (5mm x 5mm) 32-pin QFN package.**

4. Applications

- GPS Navigators
- Network Routers
- Smartphones
- Network Attached Storages (NAS)

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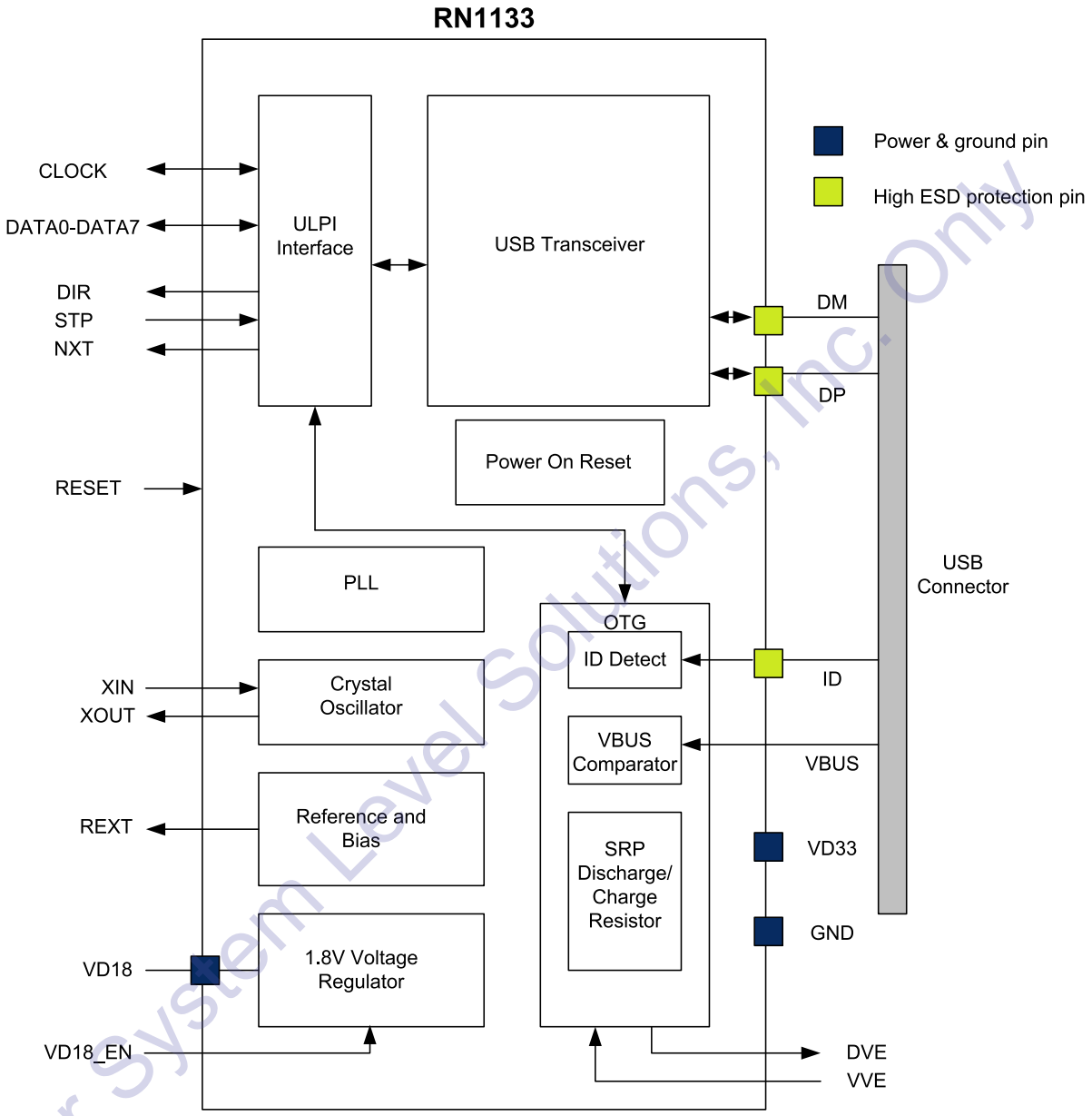

Figure 1. RN1133 Block Diagram

6. Pin Diagram

Figure 2 shows the pin definitions and locations of RN1133's QFN32 package (top view)

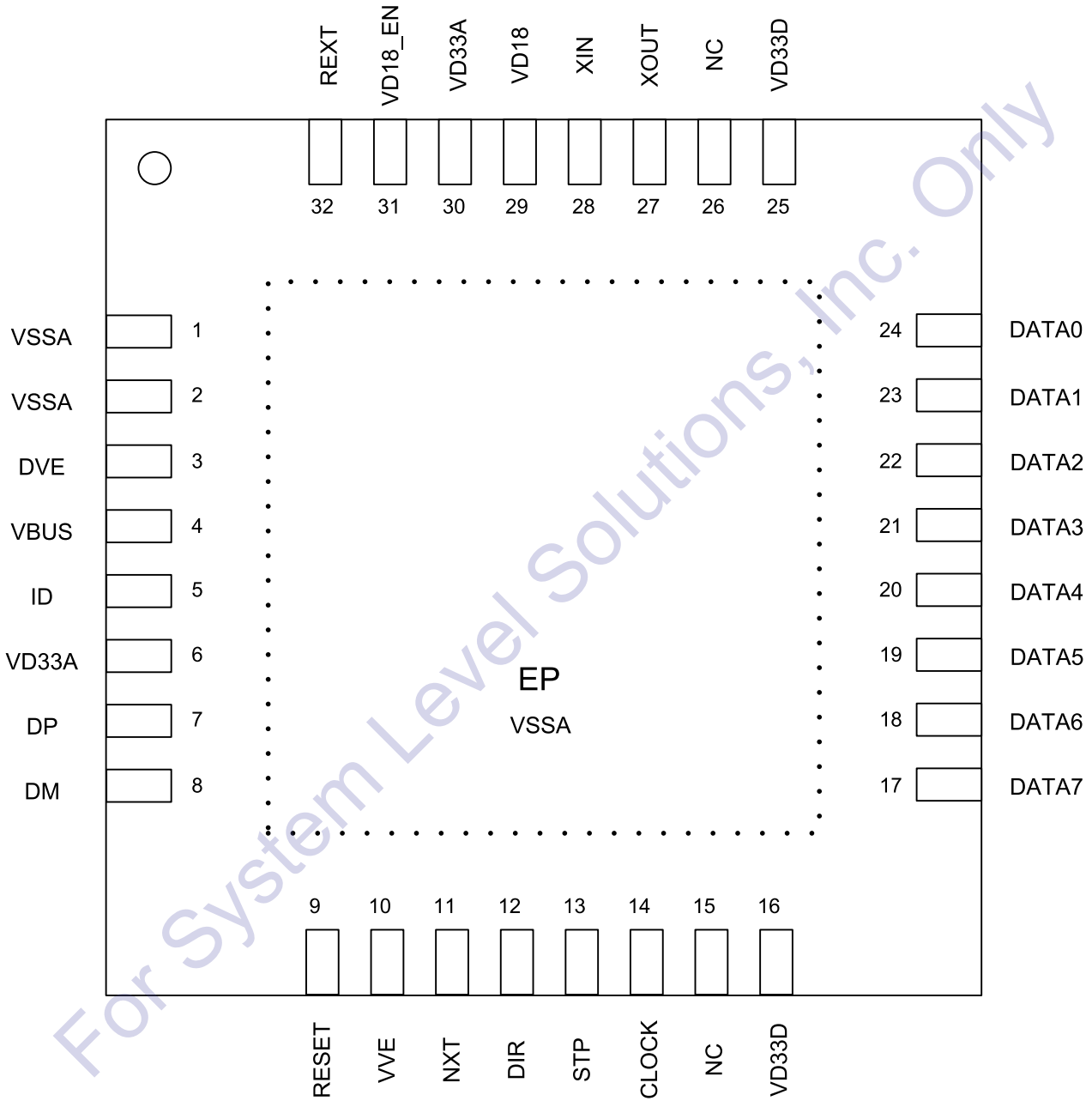

Figure 2. RN1133 Pin Diagram

7. Pin Description

Table 1. RN1133 Pin Definition

Symbol	Pin	Type	Reset State	Description
CLOCK	14	O	L	CLOCK - 60MHz ULPI clock. All interface signals are synchronous to CLOCK.
DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	24 23 22 21 20 19 18 17	IO	L	DATA[0-7] - ULPI bidirectional data bus, driven low by the Link during idle. Bus ownership is determined by DIR. The interface protection circuit for DATA[0-7] can be enabled via the **InterfaceProtectDisable** bit in the Interface Control register.
DIR	12	O	H	Direction - Controls directions of ULPI bus DATA0-DATA7. The RN1133 drives DIR high to take ownership of the bus or to indicate it can not accept data from the Link. The RN1133 drives DIR low when it has no data to transfer.
STP	13	I		Stop - The Link asserts this signal for one clock cycle to stop the data stream currently on the ULPI bus. The interface protection circuit for STP can be enabled via the **InterfaceProtectDisable** bit in the Interface Control register.
NXT	11	O	L	Next -The RN1133 asserts this signal to throttle the data.
DVE	3	O	H	Drive VBUS External – High active. This signal enables the external VBUS power switch.
VVE	10	I		VBUS Valid External - This signal should be connected to FAULT output of the external VBUS power switch or the external VBUS valid comparator. The integrated pull down register prevents floating when the exteranl power switch/comparator is not used.
RESET	9	I		Asynchronous chip reset - High active. This signal is equivalnt to the **RESET** bit in the Function Control register. The integrated pull-down resistor prevents floating when this pin is not connected.
XIN	28	I		Crystal in – 24 MHz crystal oscillator input. An external clock source can also be applied to this pin in place of the crystal.

Symbol	Pin	Type	Reset State	Description
XOUT	27	O		Crystal out – 24/19.2 MHz crystal oscillator output. This pin should not be connected when the external clock source is used.
VD18_EN	31	I		Internal 1.8V voltage regulator enable. It should be connected to pin 30 to enable the internal 1.8V regulator and be connected to ground to disable the internal 1.8V regulator. External 1.8V should be applied to VD18 pin when the internal 1.8V regulator is disabled.
REXT	32	A		Bias current setting resistor pin. It should be connected to a 20K Ohm resistor to gound.
VD18	29	A		1.8V internal regulator output.
VBUS	4	A		USB VBUS. The pin is used for the VBUS Comparator input and SRP charging/discharging.
ID	5	A		USB ID. This pin should be 0 for an OTG A-Device and 1 for an OTG B-Device. For non-OTG applications, the pin can be floated.
DM	8	A		USB D-.
DP	7	A		USB D+.
VD33A	6, 30	A		3.3V power for analog blocks.
VD33D	16,25	A		3.3V power for digital blocks.
VSSA	1, 2	A		Ground pin for analog blocks.
NC	15, 26	NC		No connection. Reserved for future usage.
VSSD	EP	A		Ground pin for digital blocks (including 1.8V, 3.3V digital circuitry).
Note: EP - Exposed Paddle (bottom of the package) to be connected to board ground plane.				

8. Function Description

8.1 ULPI Interface

The RN1133's 12 pin ULPI interface is compliant with the industrial standard UTMI+ Low Pin Interface (ULPI) Specification Rev1.1 and provides a glueless interface to the Link processor. The RN1133's ULPI compliant register set allows the Link to transmit and receive USB data, control over USB host, OTG, peripheral functionalities, and select the operation mode. An external VBUS power switch can also be controlled via the ULPI register for USB VBUS monitoring, charging and discharging required in the OTG operation. The RN1133's ULPI interface can be configured into Synchronous, Low Power, 6-Pin FsLsSerial, 3-Pin FsLsSerial and Carkit modes for various applications.

8.1.1 Synchronous Mode

This is the default mode of operation. While the clock is running and stable, the ULPI interface carries commands and data that are synchronous to CLOCK. Table 2 shows the signal definition of Synchronous Mode.

Table 2. ULPI Synchronous Mode Pin Definition

Signal	Direction	Description
CLOCK	OUT	60MHz interface clock. All interface signals are synchronous to CLOCK.
DATA[7:0]	I/O	Bi-directional data bus. Driven low by the Link during idle. Bus ownership is determined by DIR. The Link and RN1133 initiate data transfers by driving a non-zero pattern onto the data bus. The single edged data is transferred with respect to rising edge of CLOCK.
DIR	OUT	Direction. Controls the direction of the DATA bus. When the RN1133 has data to transfer to the Link, it drives DIR high to take ownership of the bus. When the RN1133 has no data to transfer it drives DIR low and monitors the bus for Link activity. The RN1133 drives DIR high whenever the interface cannot accept data from the Link.
STP	IN	Stop. The Link asserts this signal for 1 clock cycle to stop the data stream currently on the bus. If the Link is sending data to the RN1133, STP indicates the last byte of data was on the bus in the previous cycle. If the RN1133 is sending data to the Link, STP forces the RN1133 to end its transfer, de-assert DIR and relinquish control of the data bus to the Link.
NXT	OUT	Next. The RN1133 asserts this signal to throttle the data. When the Link is sending data to the RN1133, NXT indicates when the current byte has been accepted by the RN1133. The Link places the next byte on the data bus in the following clock cycle. When the RN1133 is sending data to the Link, NXT indicates when a new byte is available for the Link to consume.